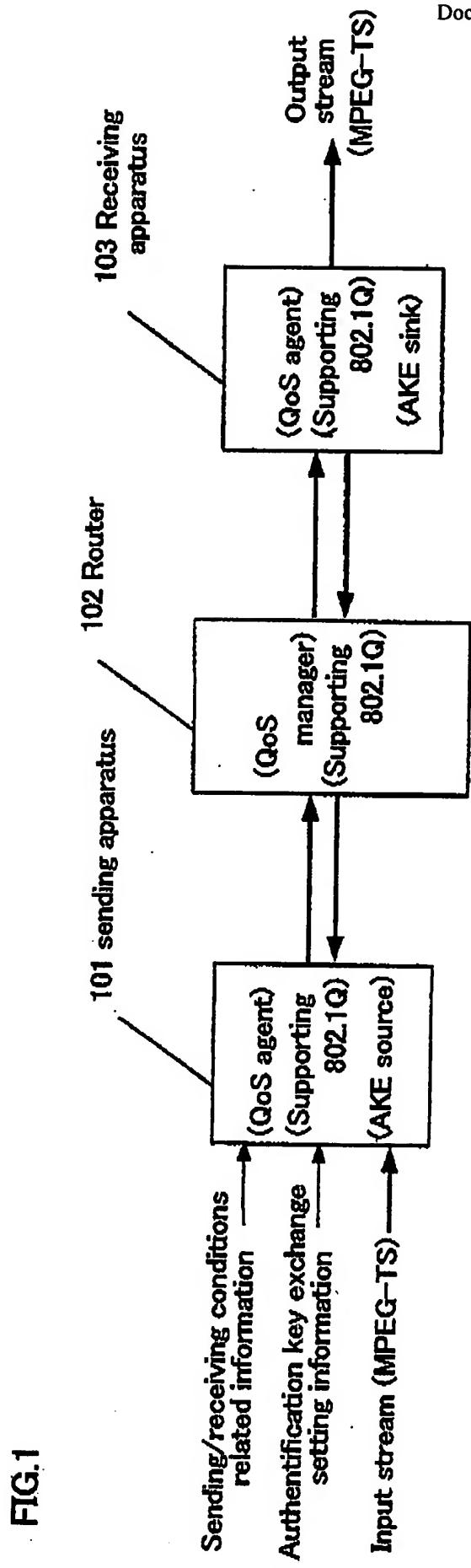


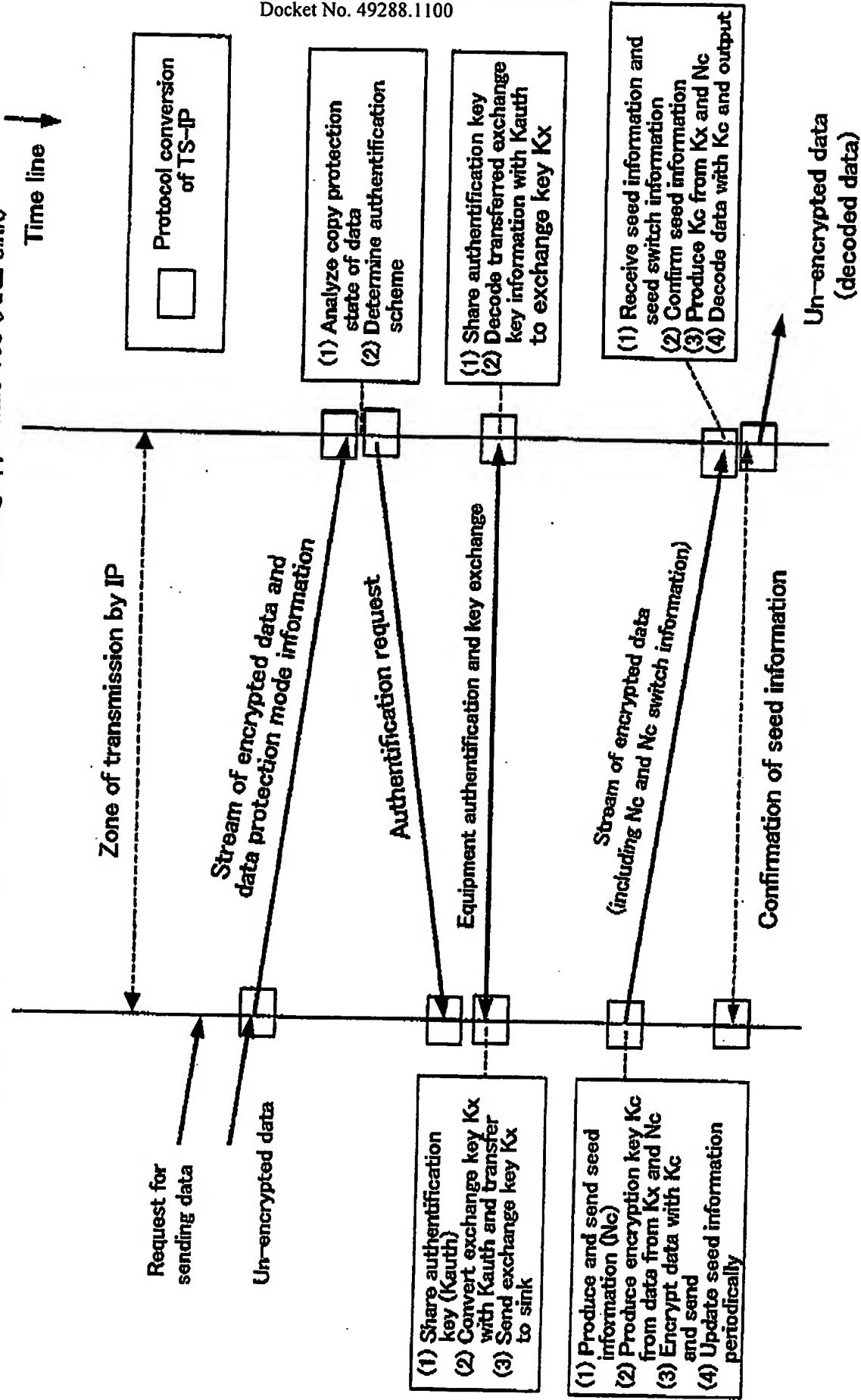
10/531713



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FIG.2 Sending apparatus 101 (AKE source)

Receiving apparatus 103 (AKE sink)



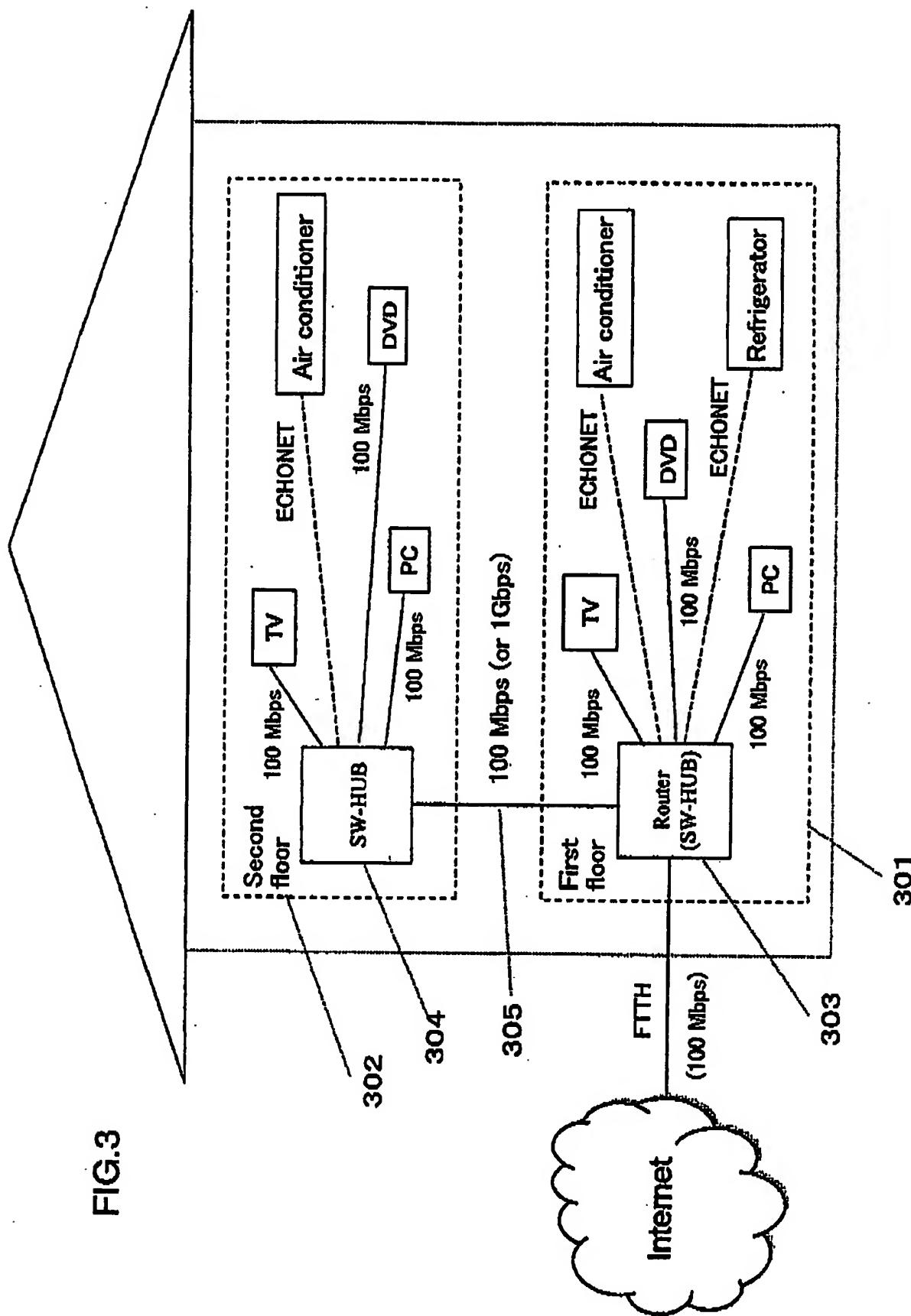
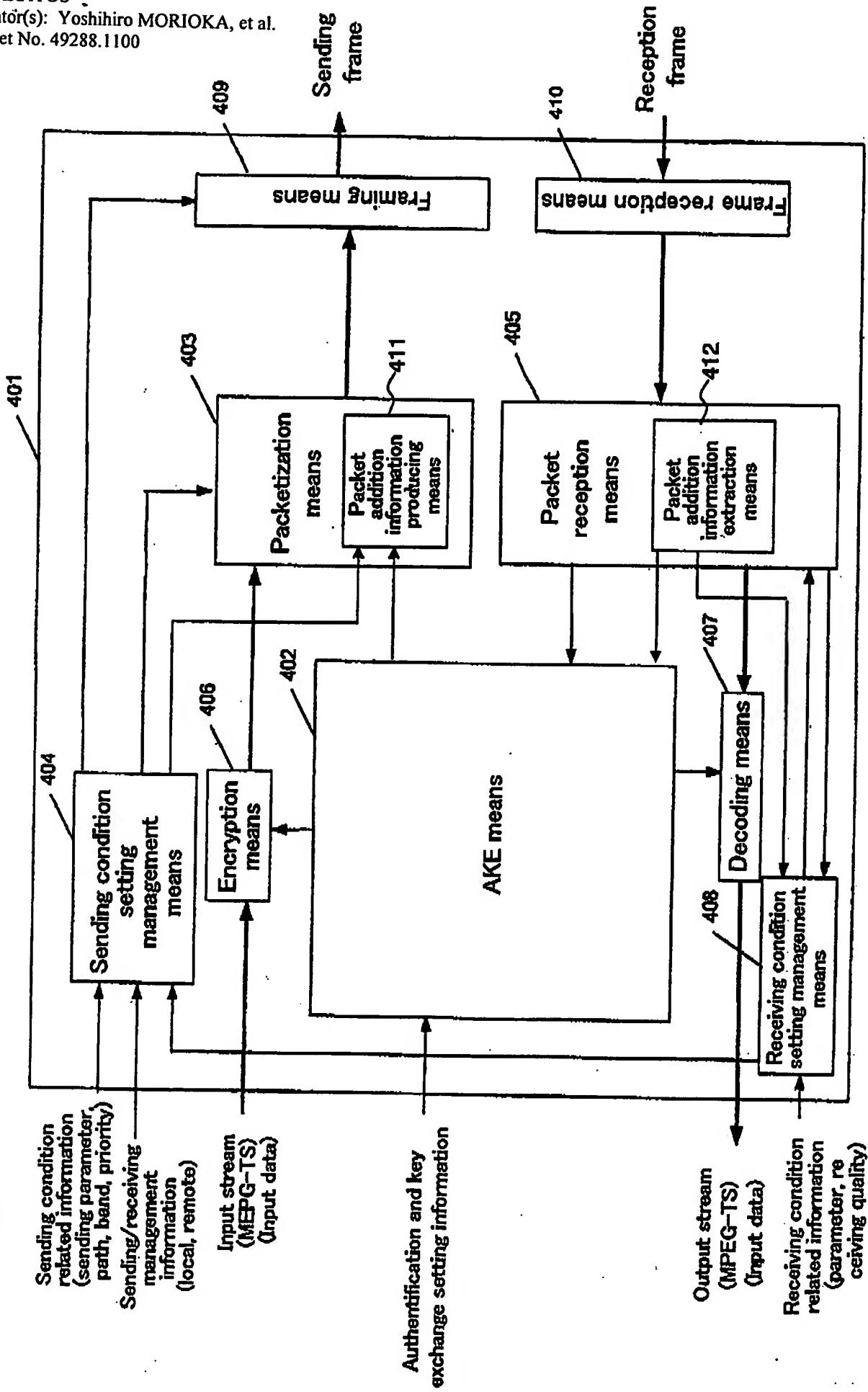


FIG.3

Title: PACKETS SENDING/RECEIVING APPARATUS  
 Inventor(s): Yoshihiro MORIOKA, et al.  
 Docket No. 49288.1100

FIG.4



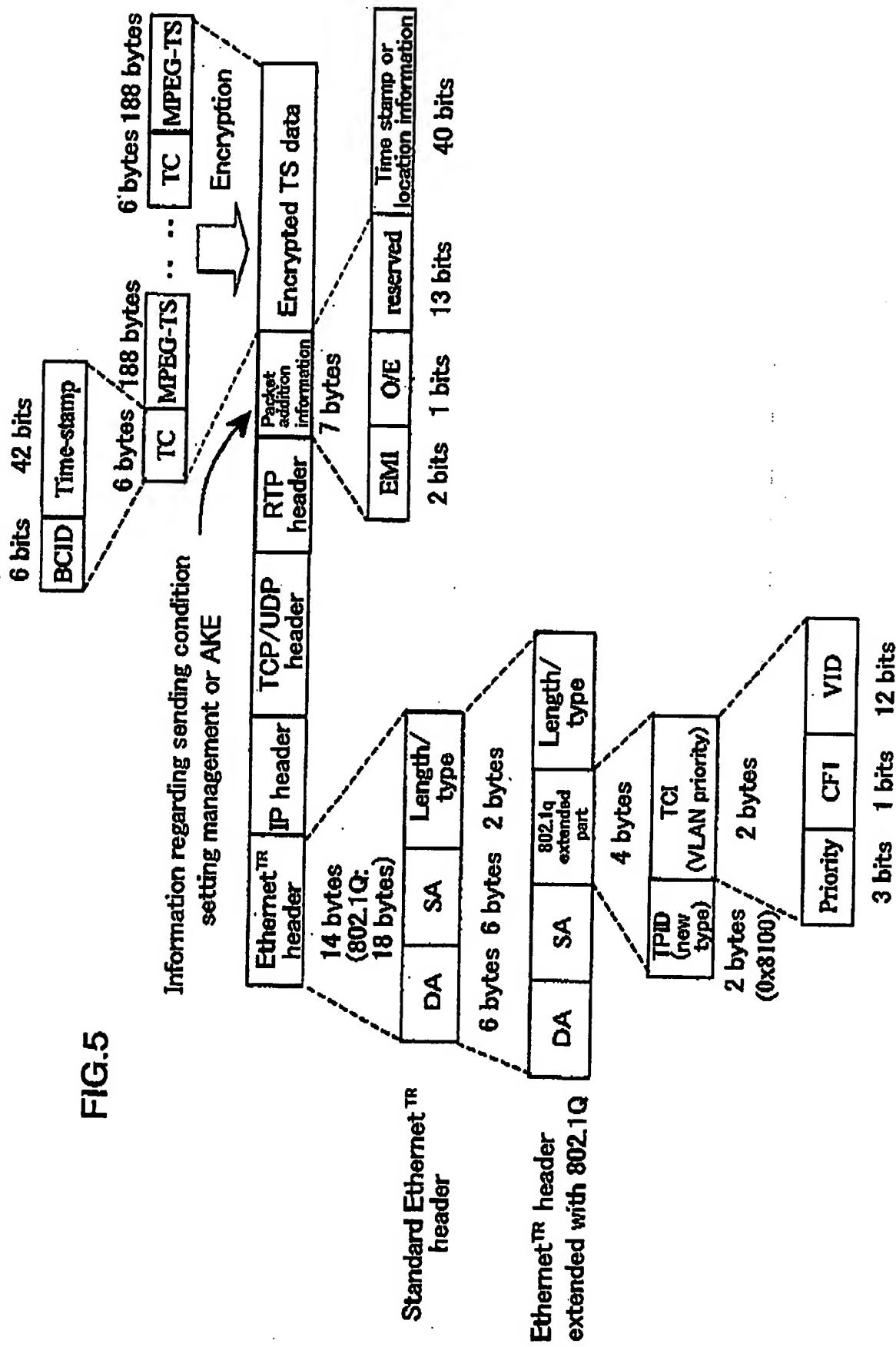


FIG.6

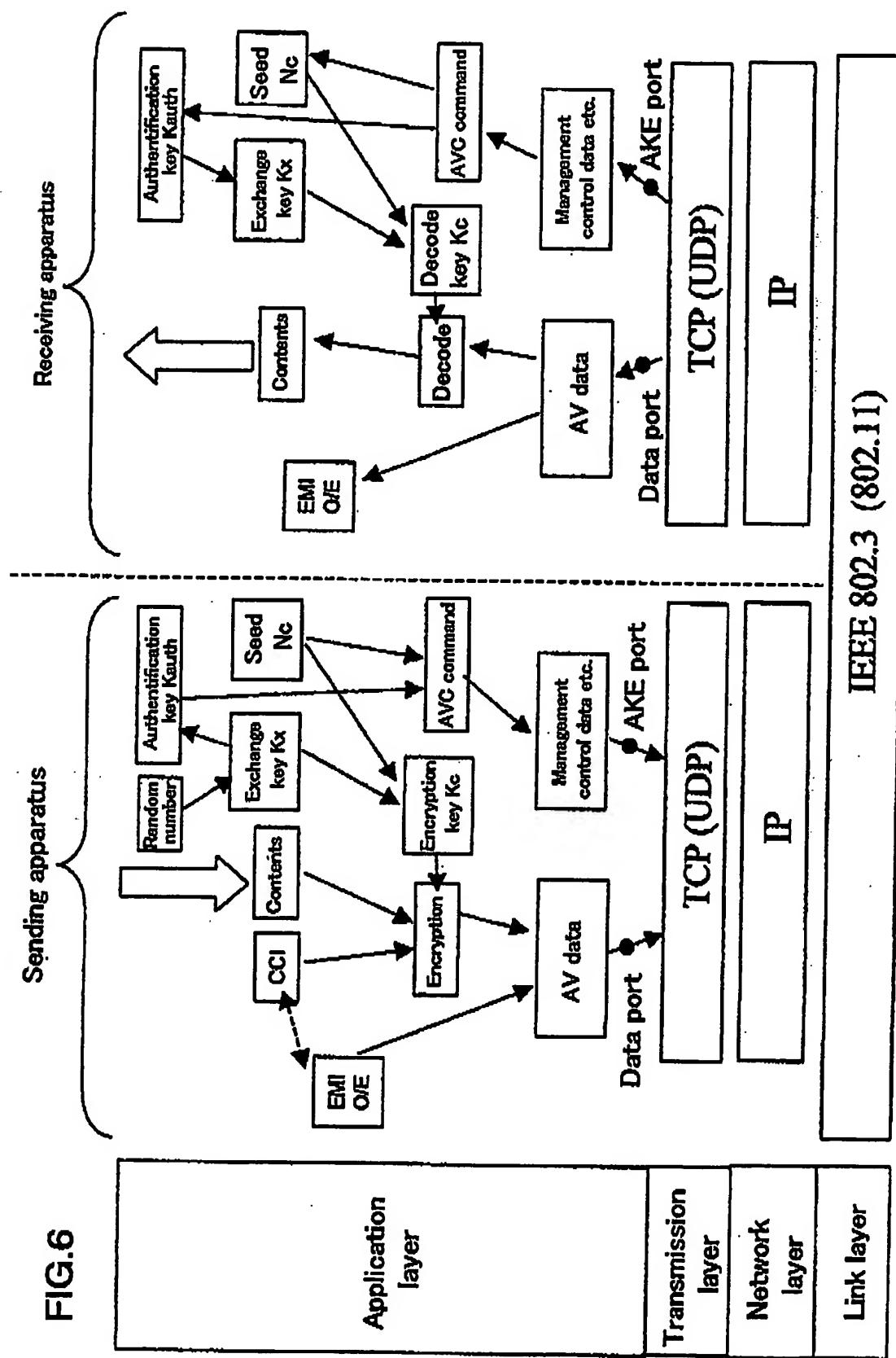


FIG. 7

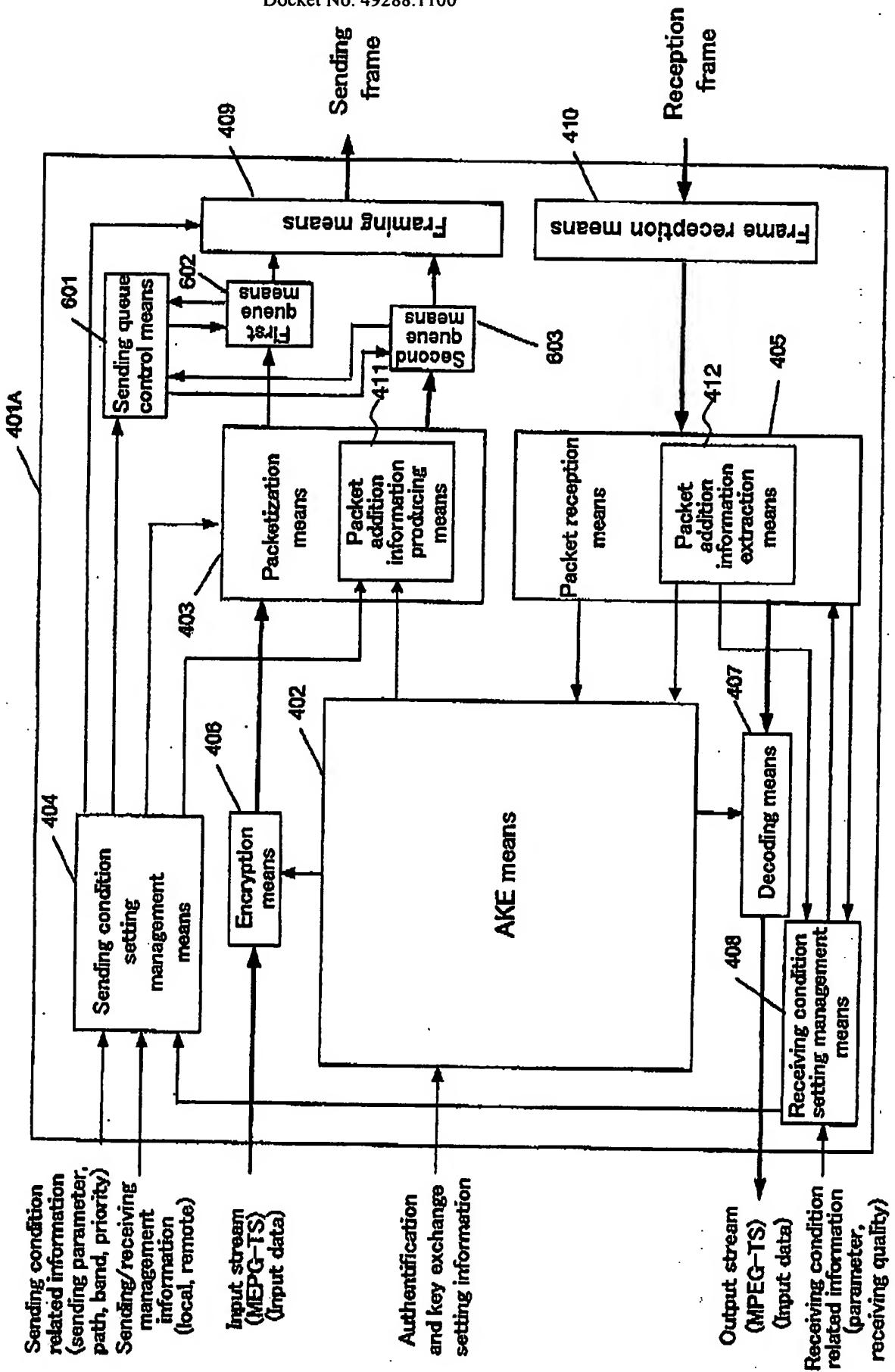
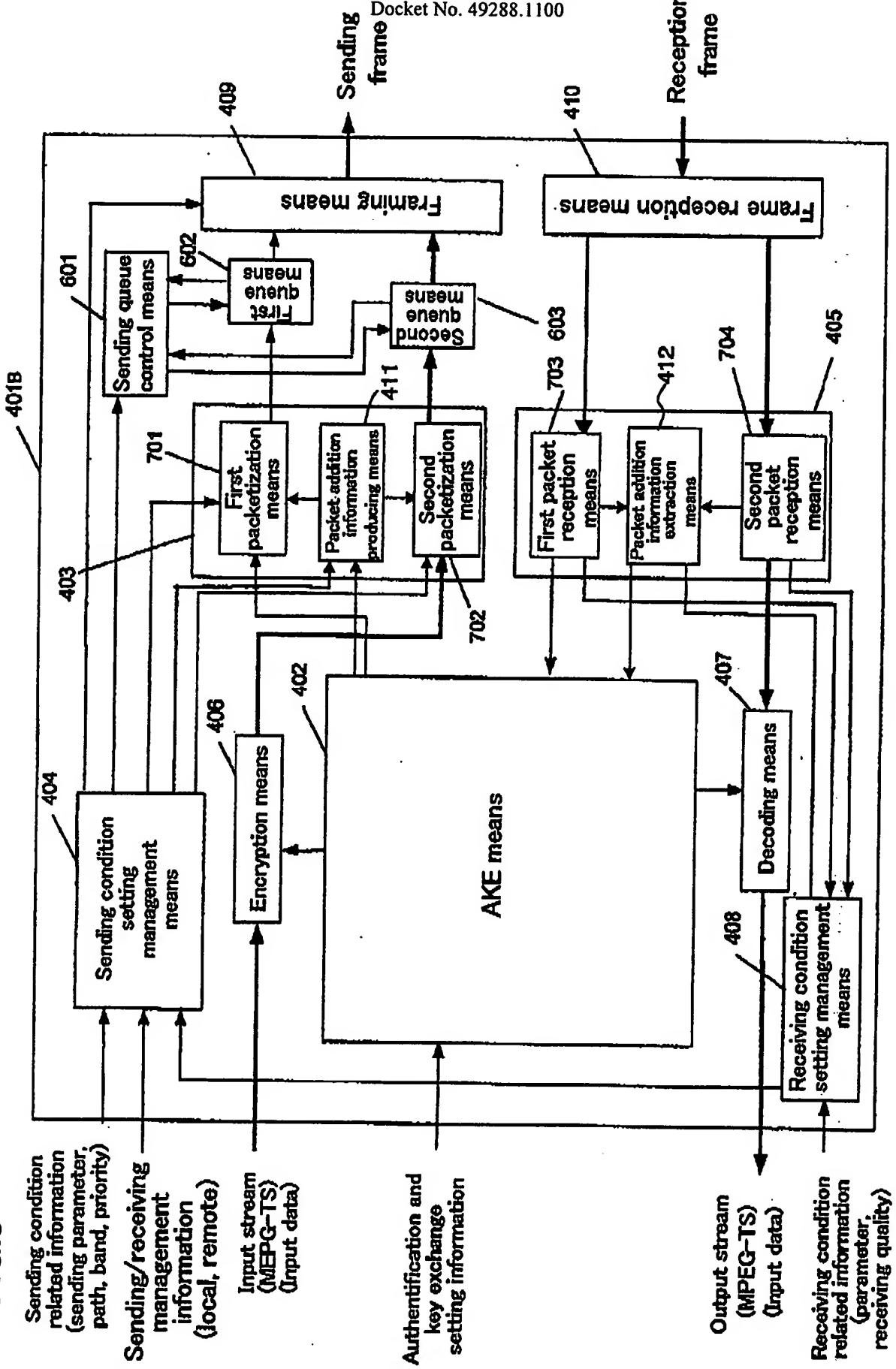
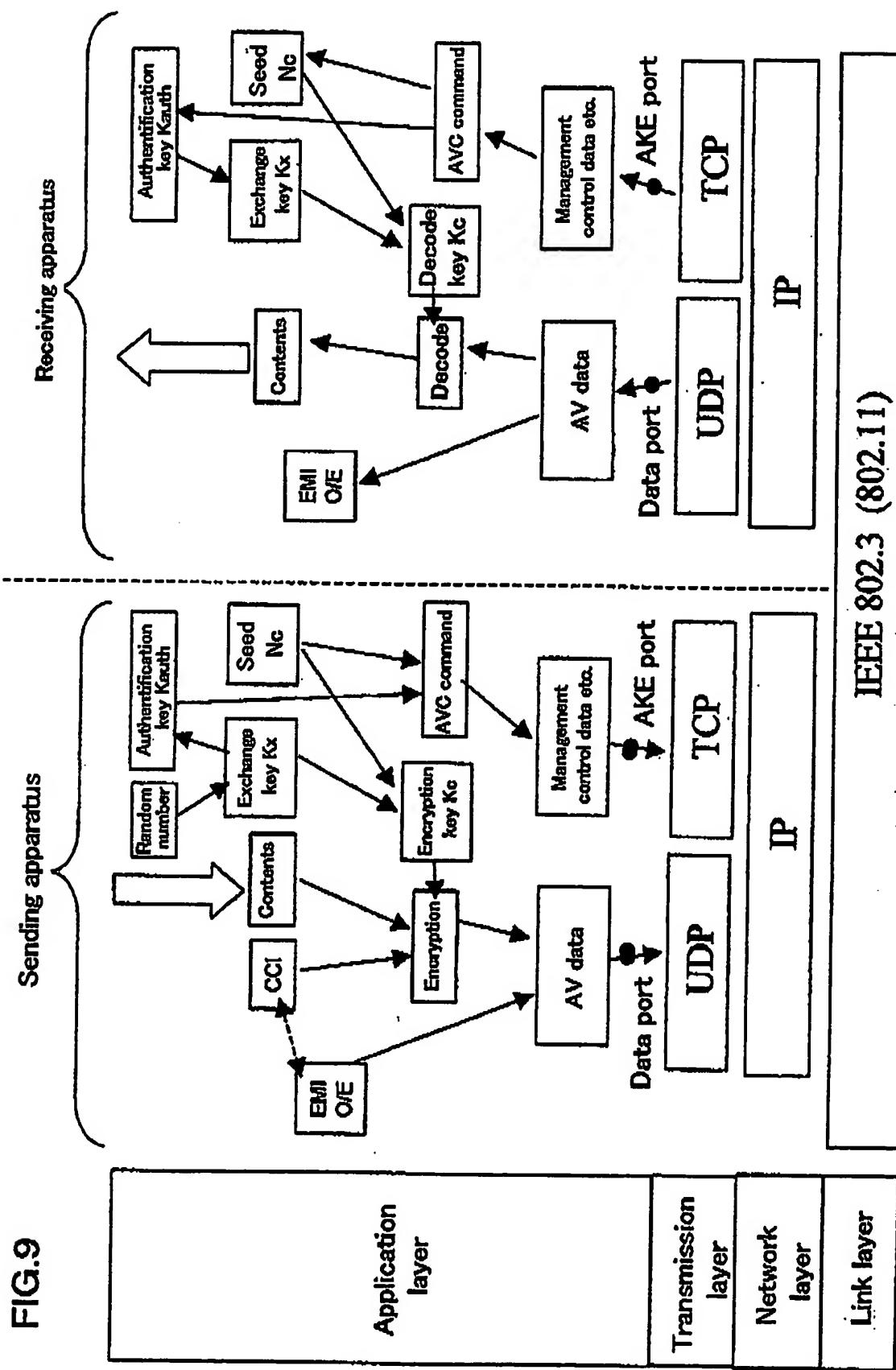


FIG. 8





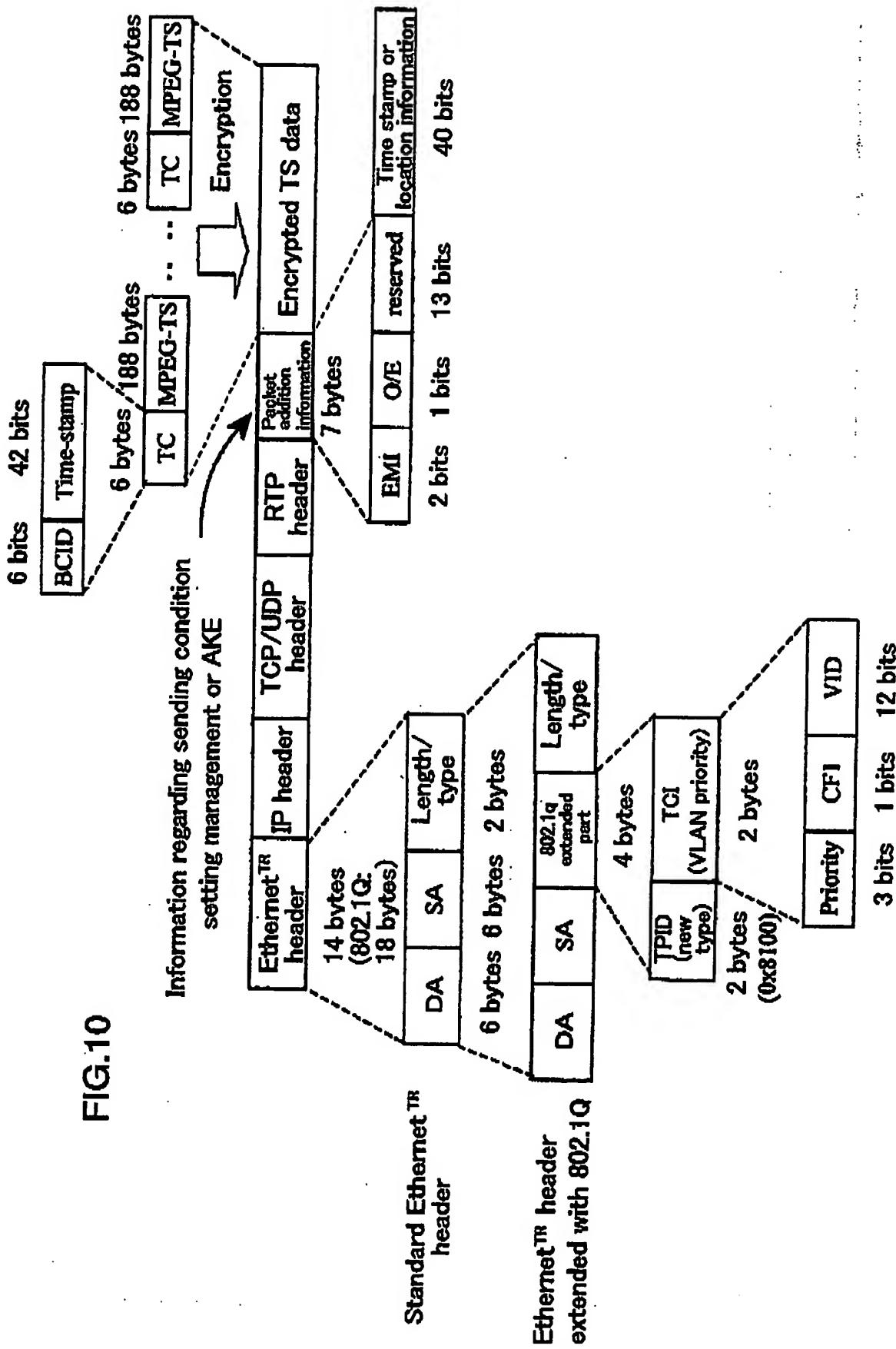
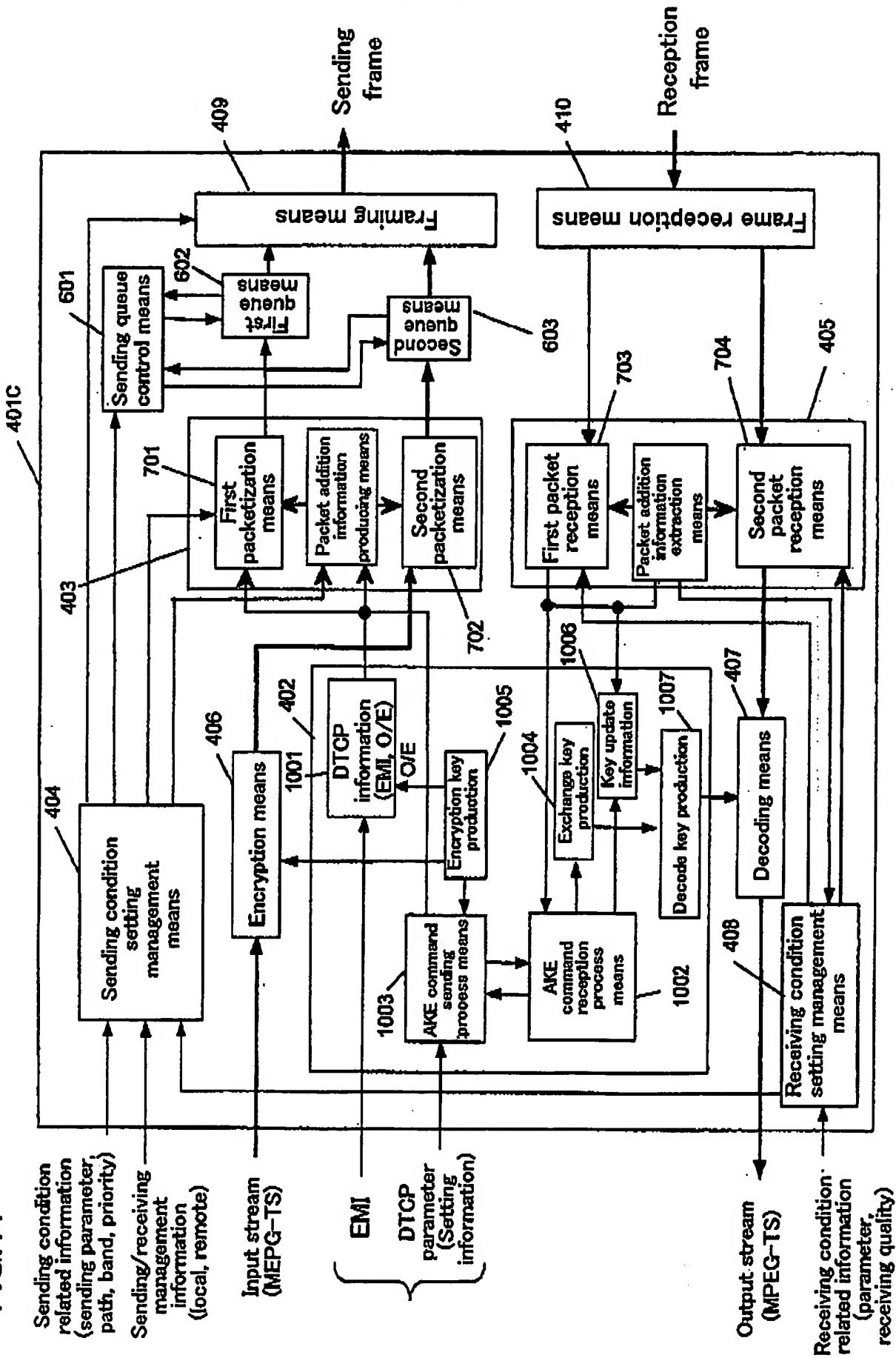
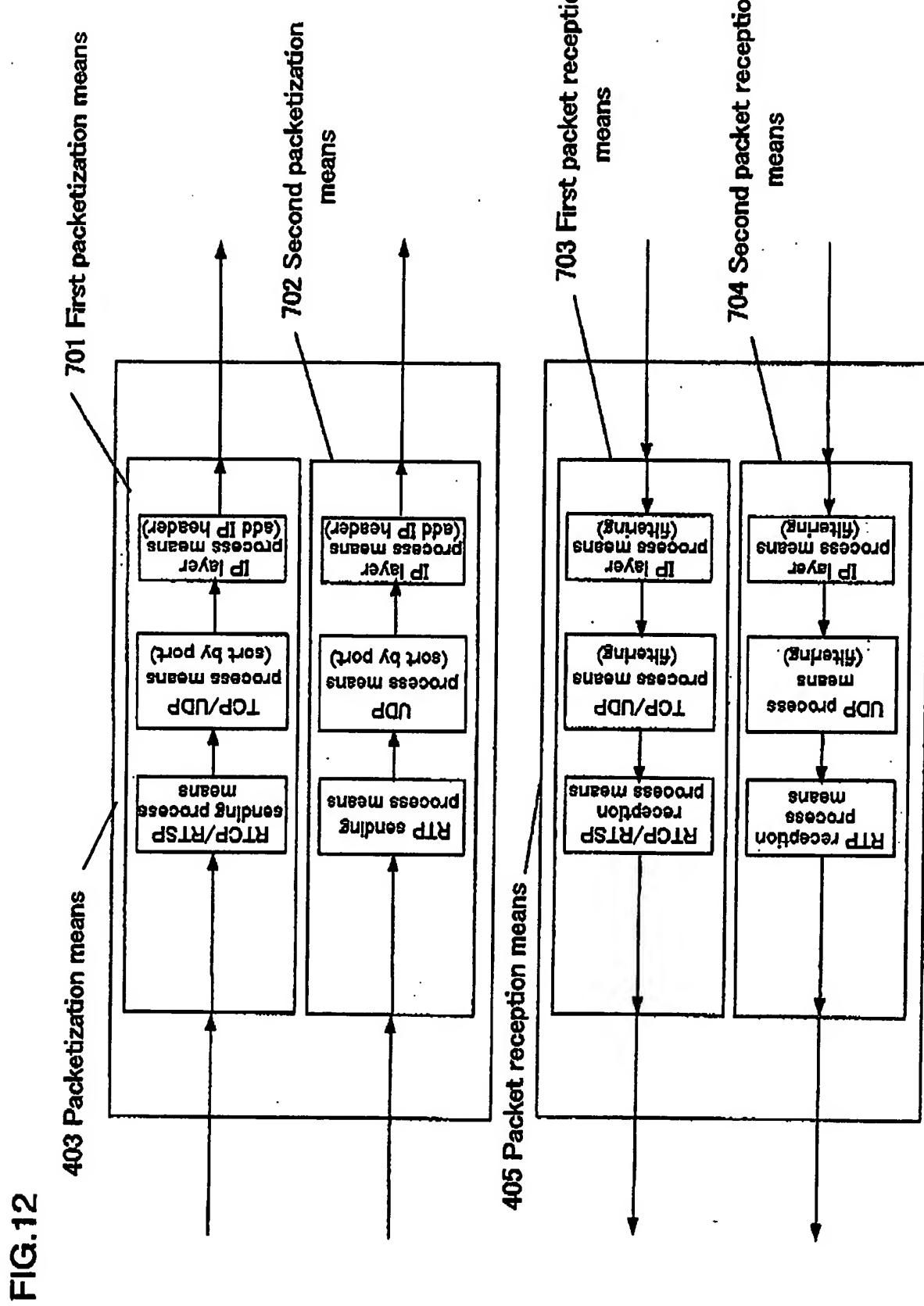


FIG. 11





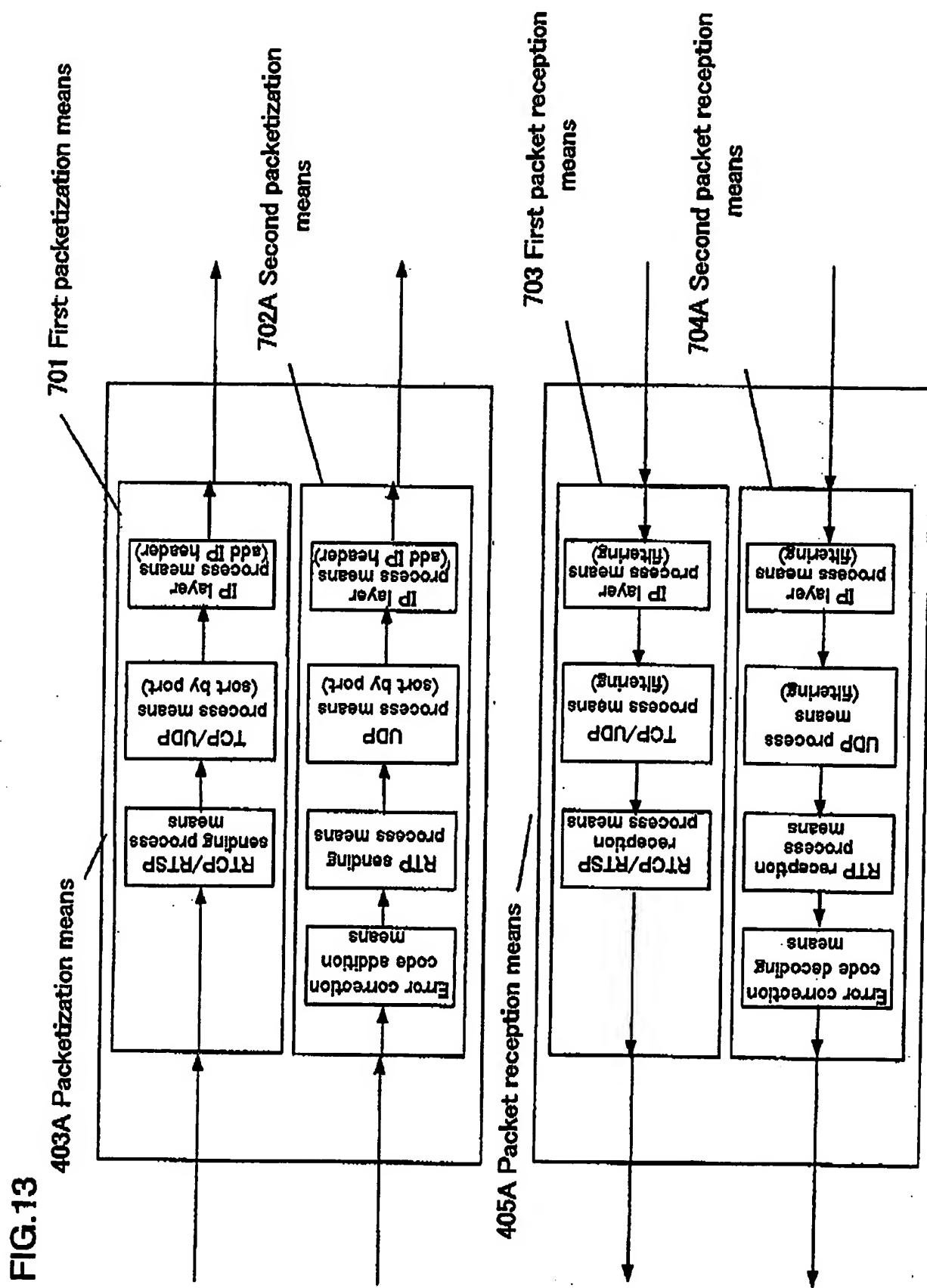
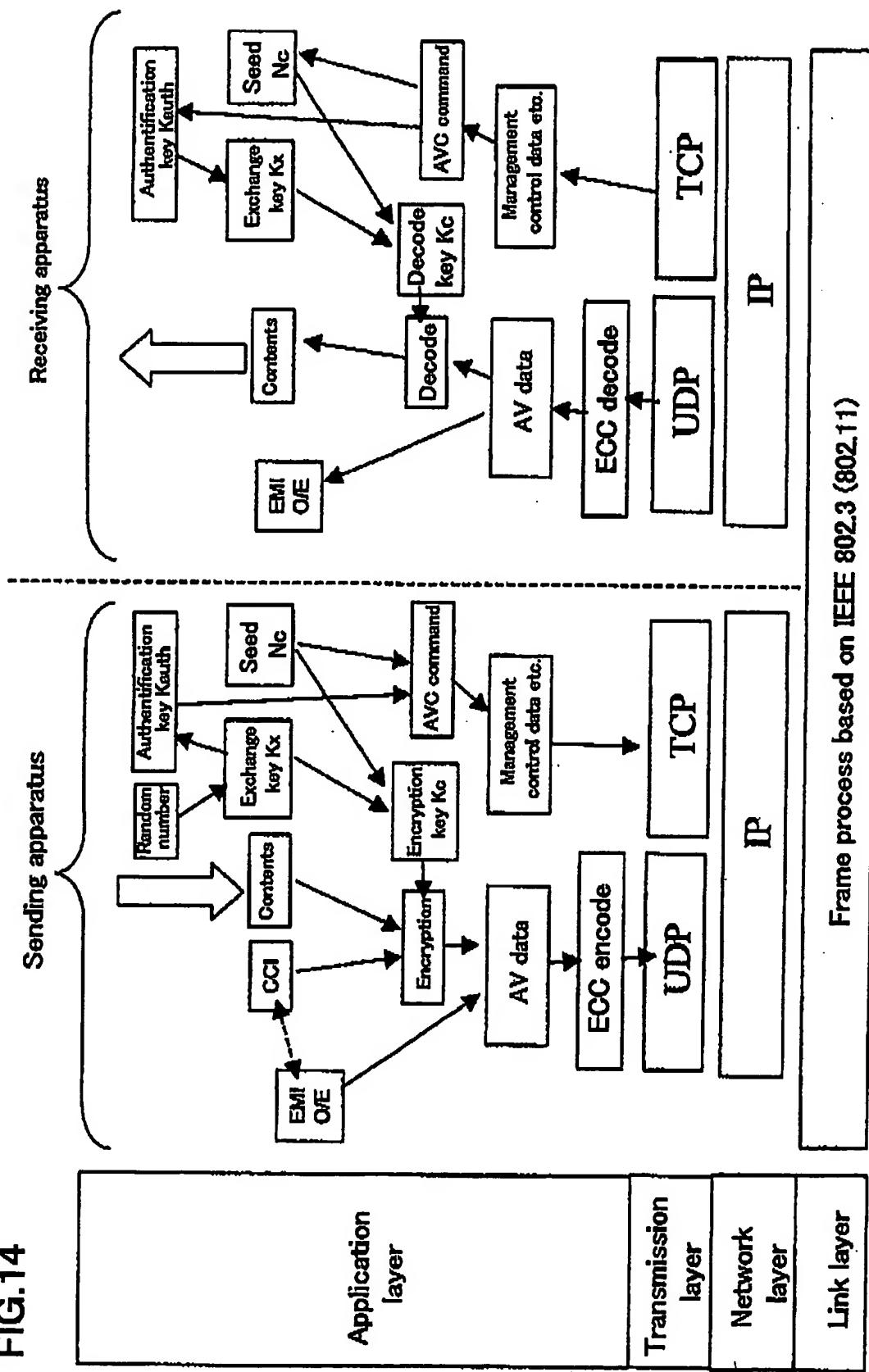


FIG.13

FIG.14



(Explanation using OSI model)

Frame process based on IEEE 802.3 (802.11)

Fig. 15

Example where error correction addition means is Reed-Solomon code

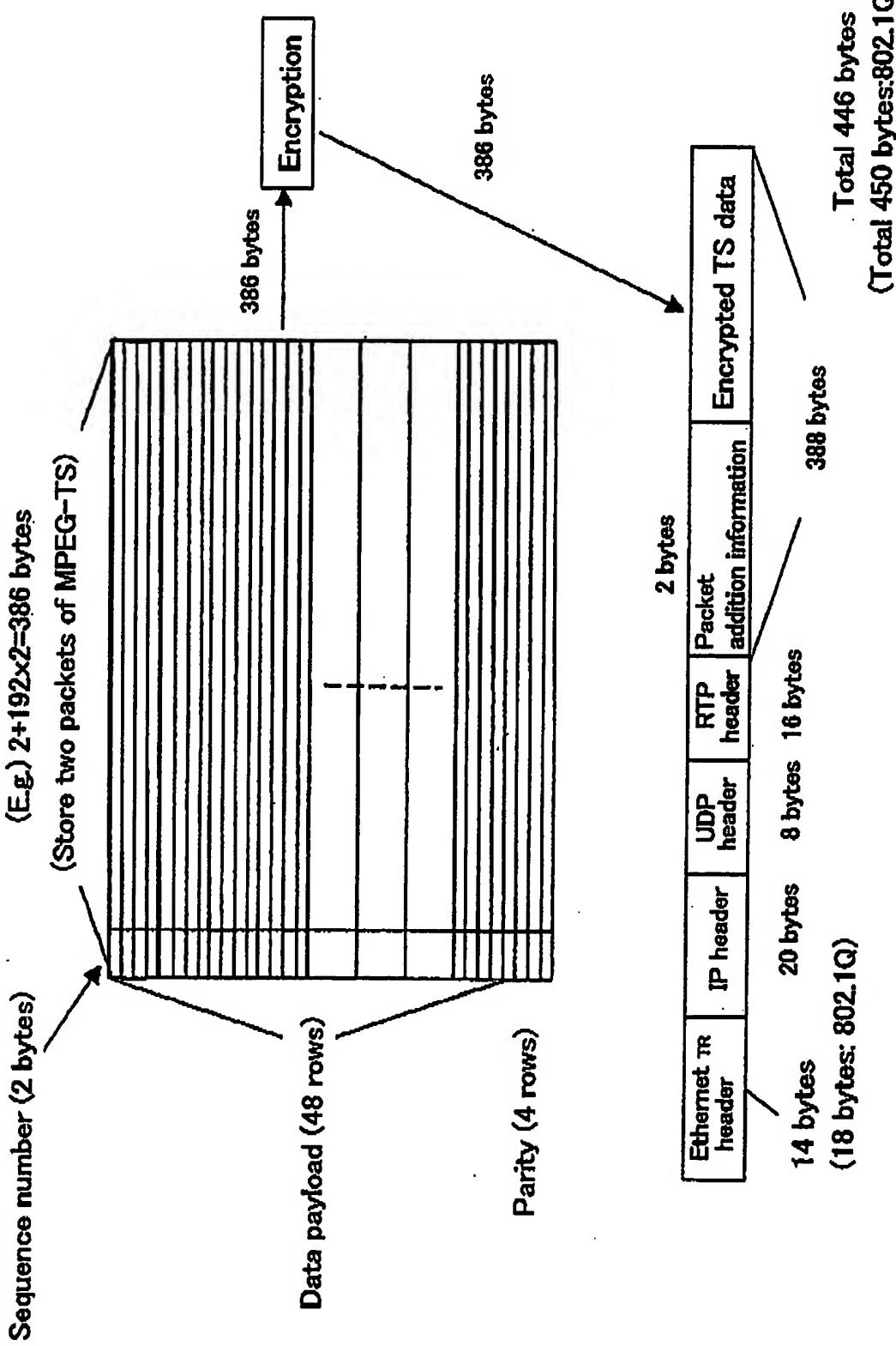


Fig. 16 Example where error correction addition means is parity

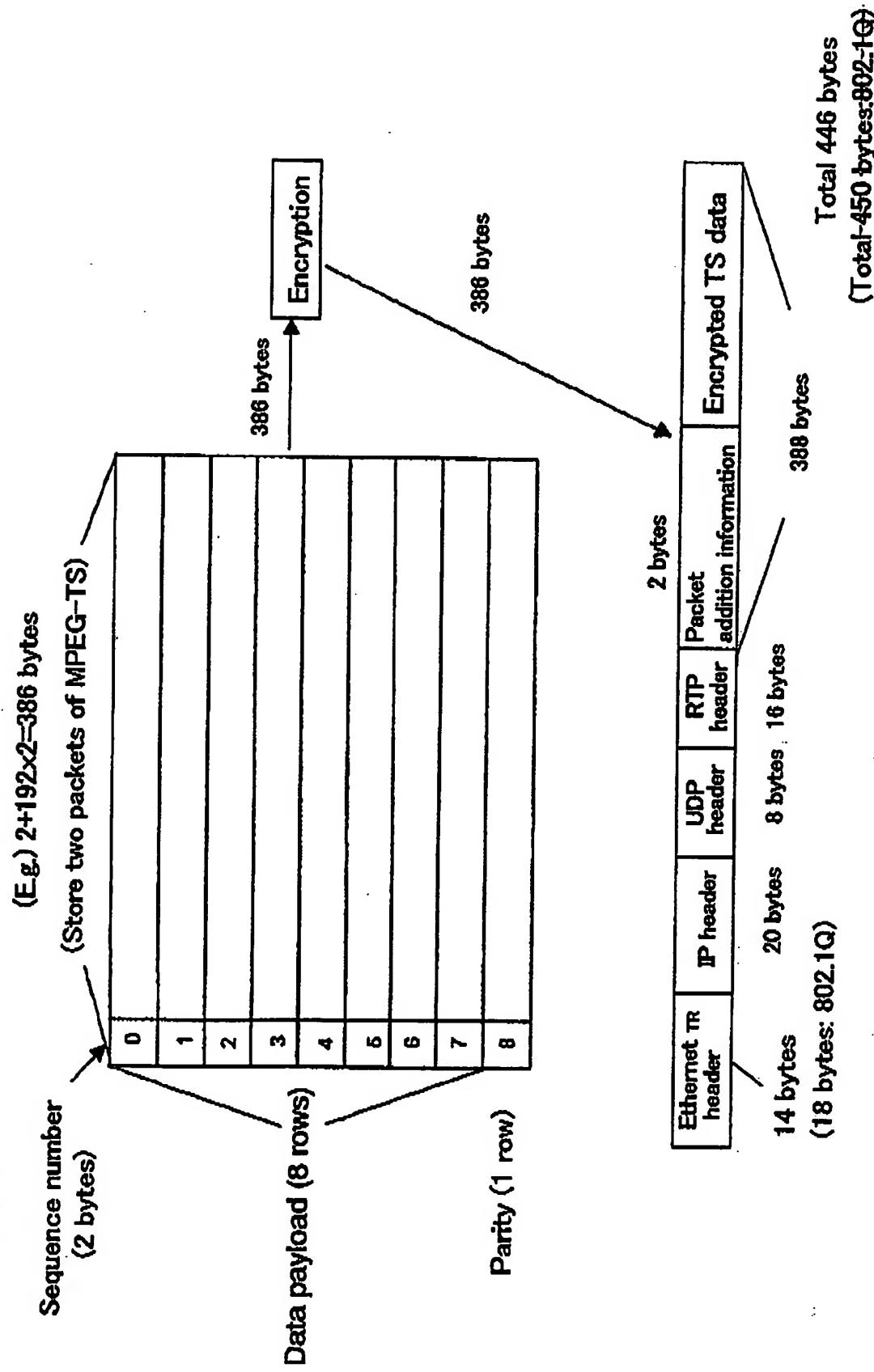


FIG.17

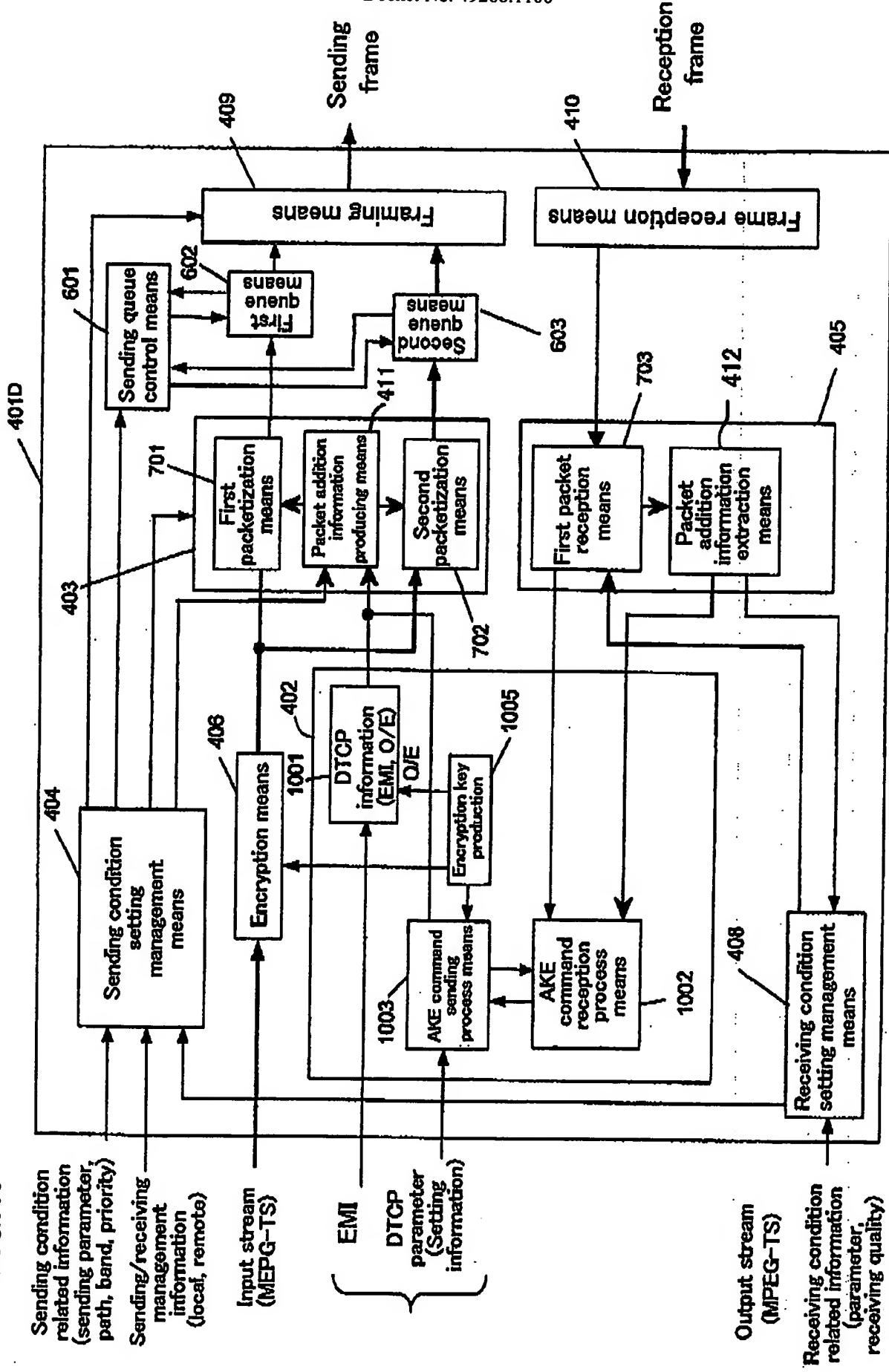
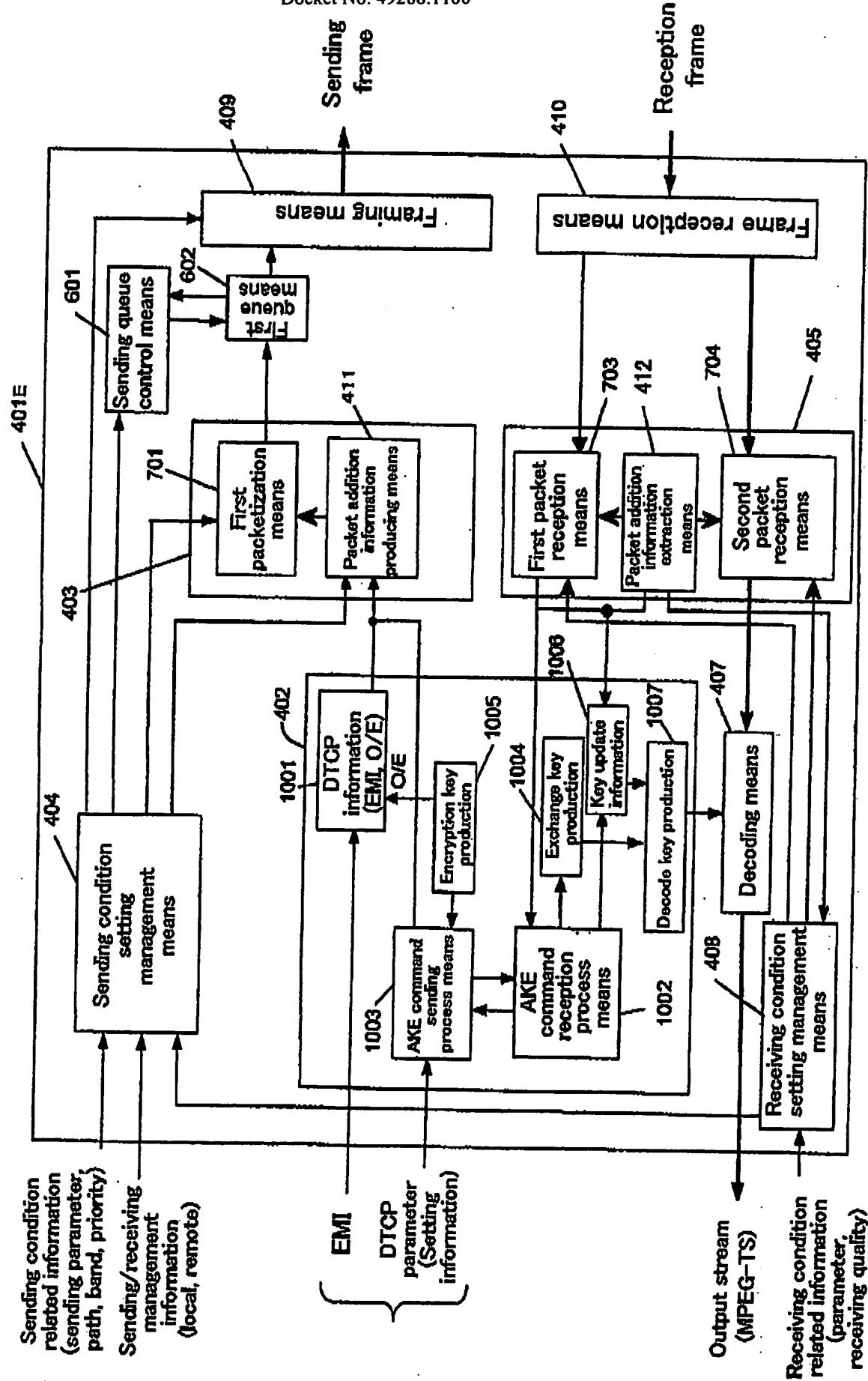


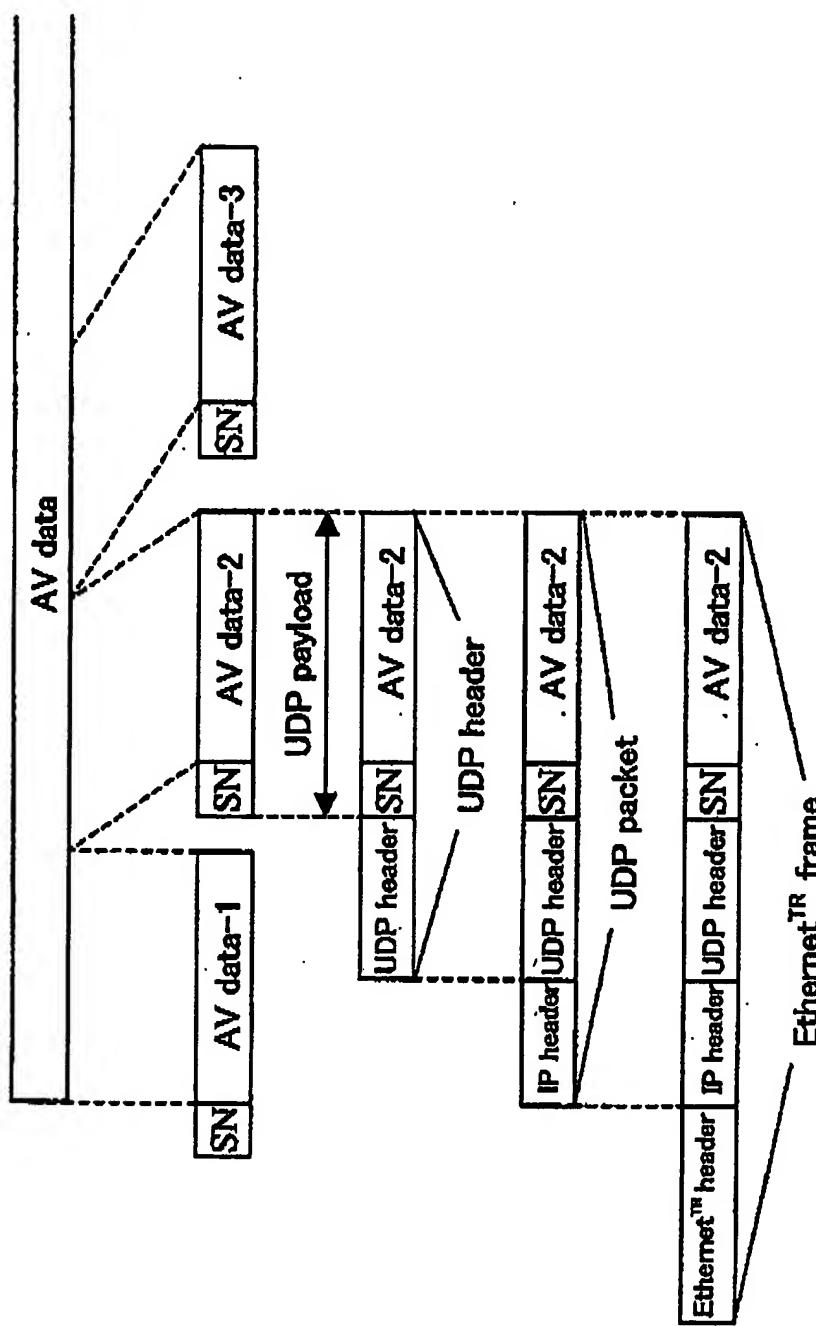
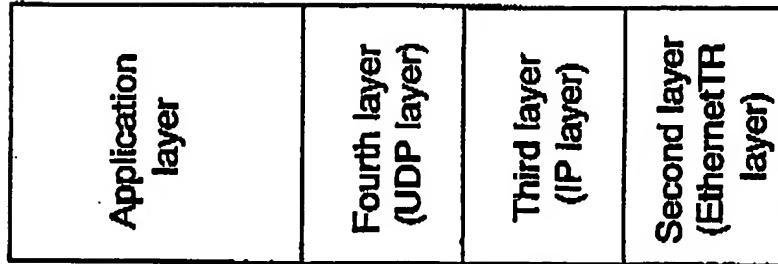
FIG.18



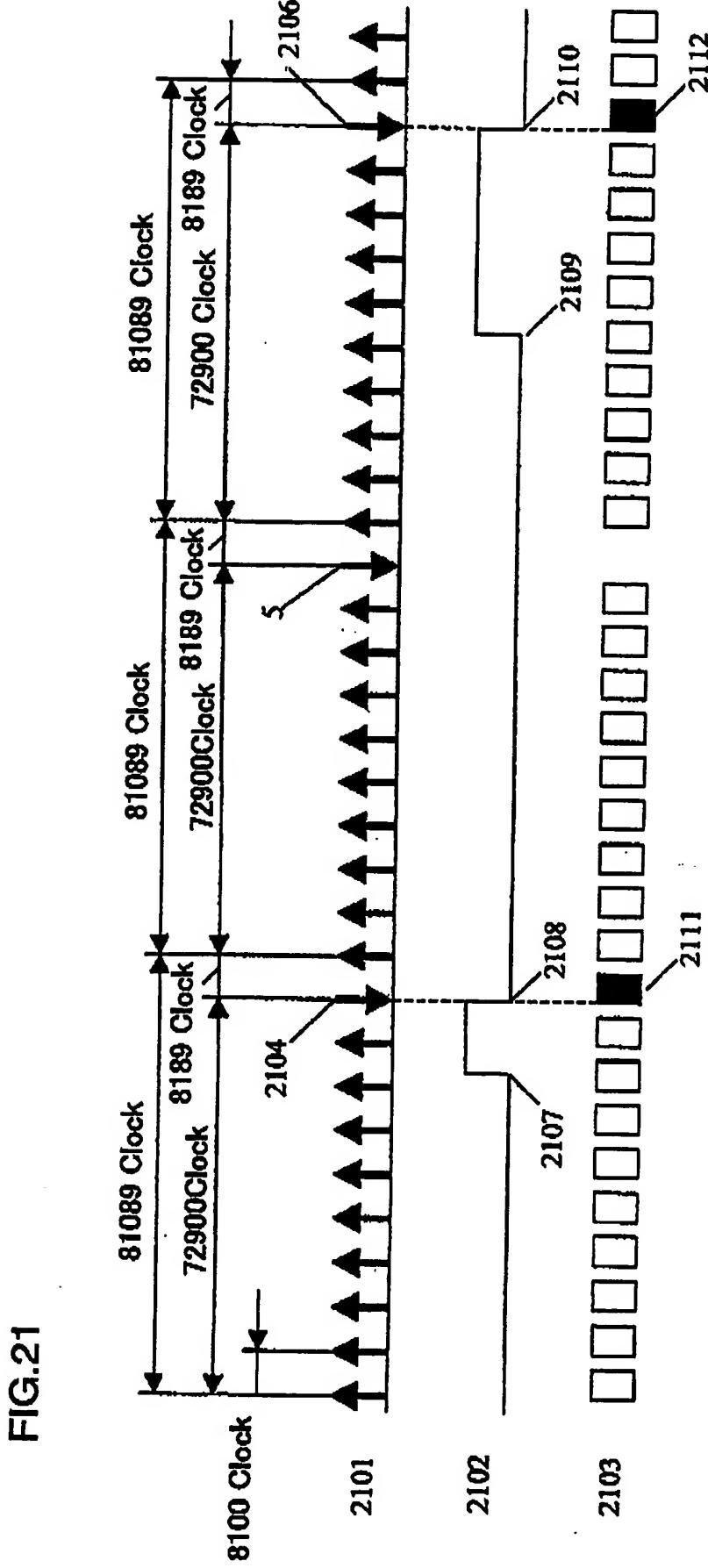
Block diagram illustrating the architecture of a data processing system for frame data sending:

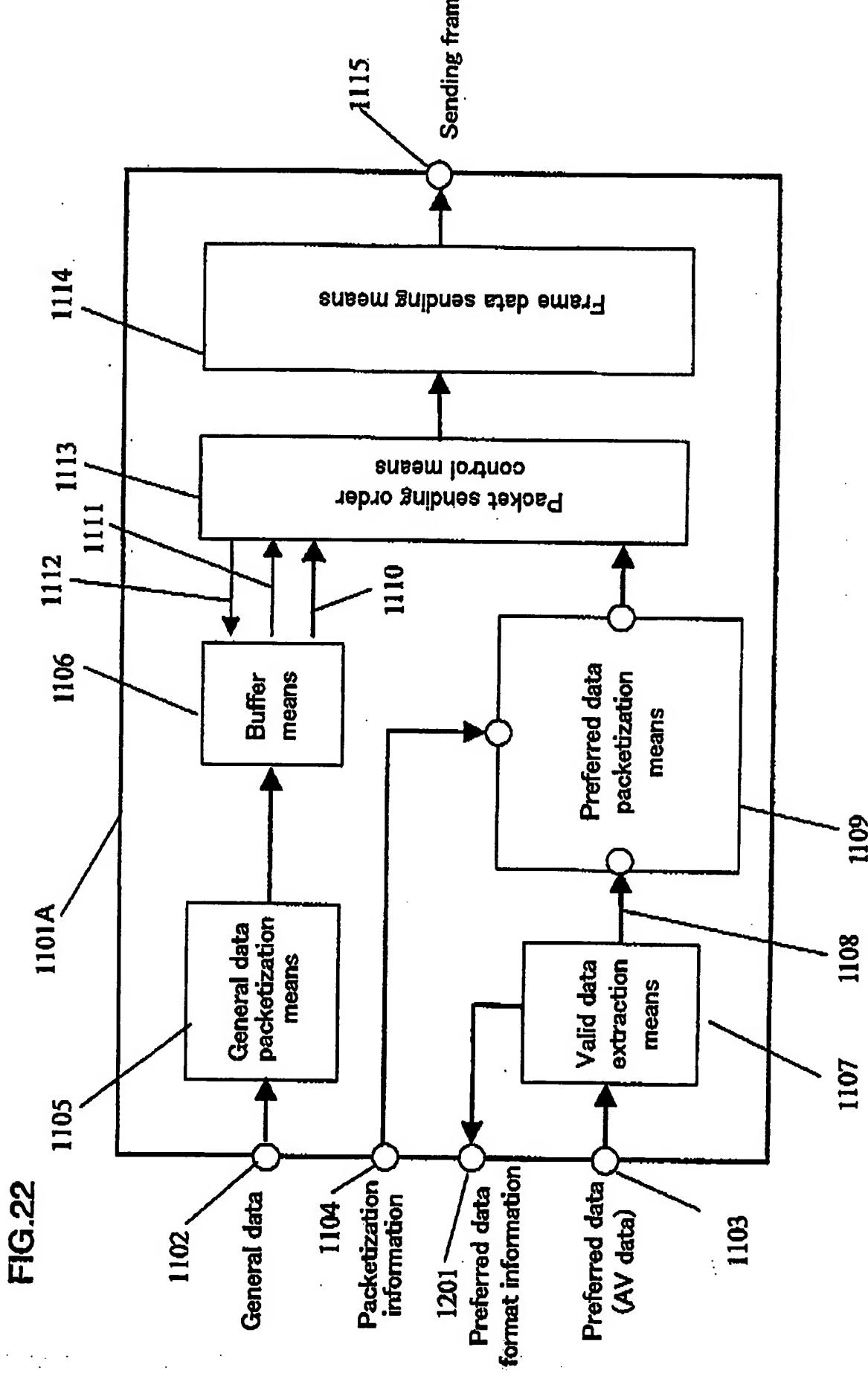
- Frame data sending means** (1114) is the central component, receiving a **Sending frame** signal (1115) and sending it to the outside.
- Packet sending order control means** (1112) is influenced by several components:
  - Buffer means** (1106) and **General data packetization means** (1101) provide input to the control means.
  - Preferred data packetization means** (1108) and **Valid data extraction means** (1107) also provide input to the control means.
  - General data** (1102) and **Packetization information** (1104) are input to the general data packetization means.
  - Preferred data (AV data)** (1103) is input to the valid data extraction means.
- Valid data extraction means** (1107) and **Preferred data extraction means** (1108) are connected to the control means.

FIG.20



(Representation using OSI model)





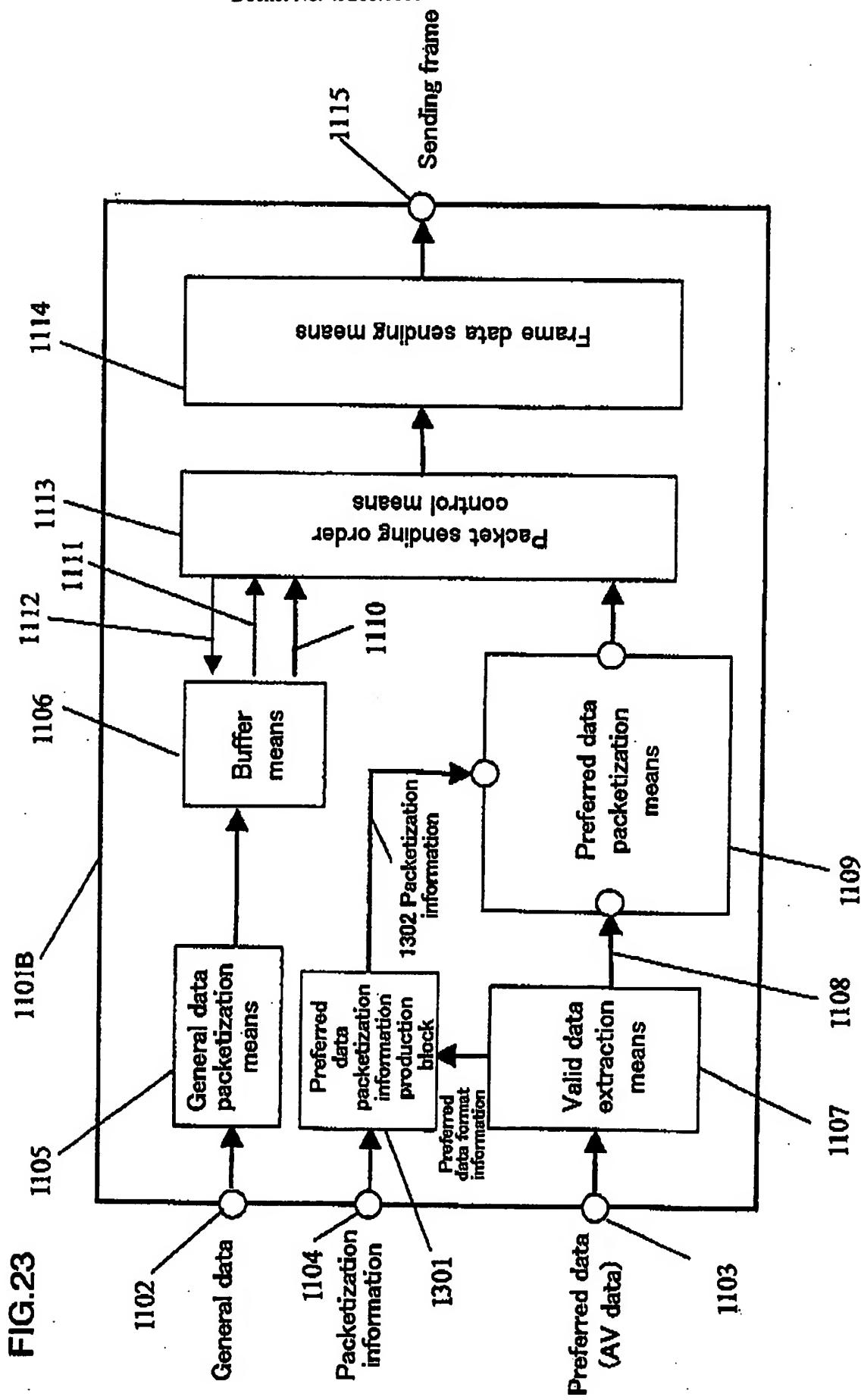


FIG.24

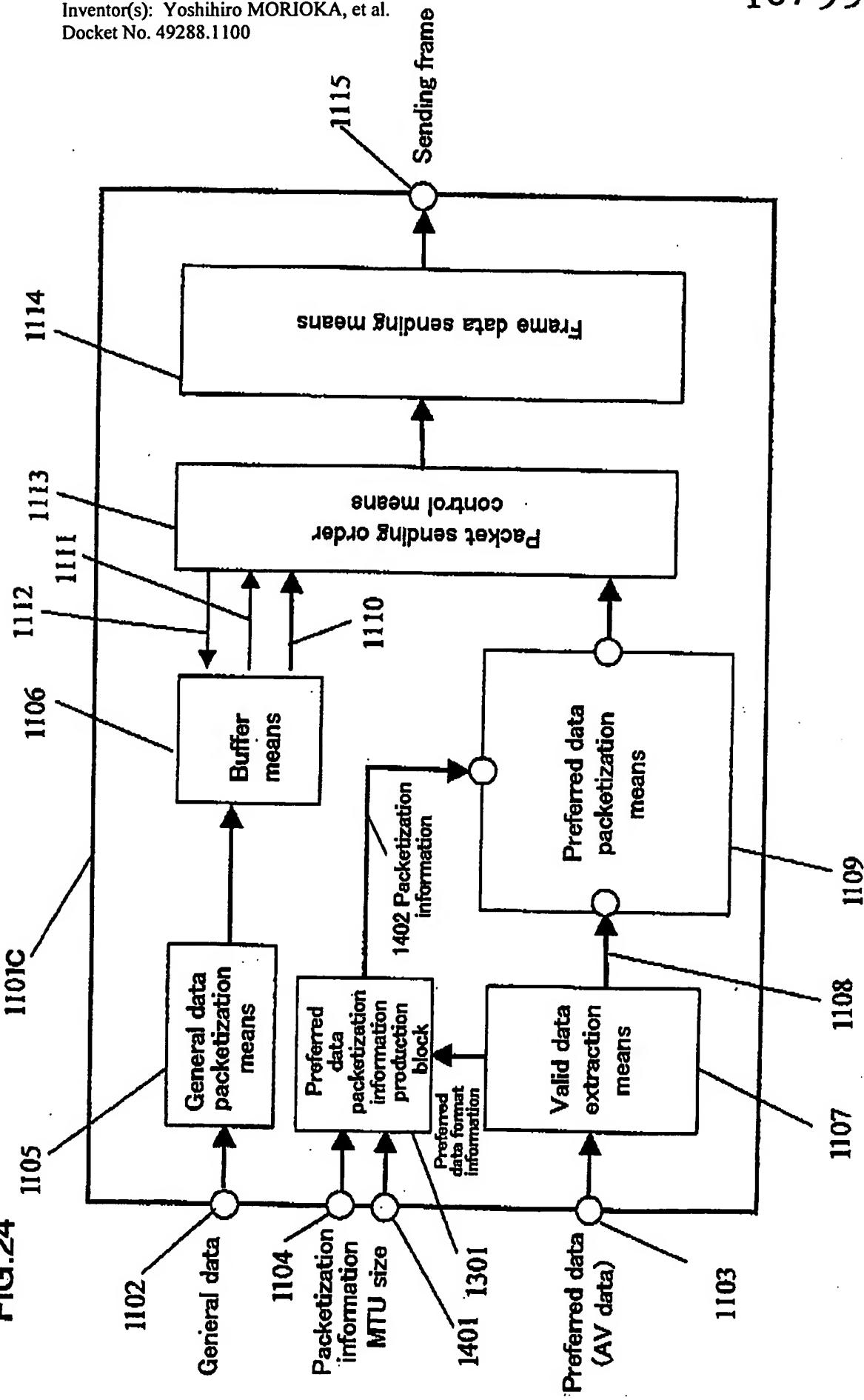
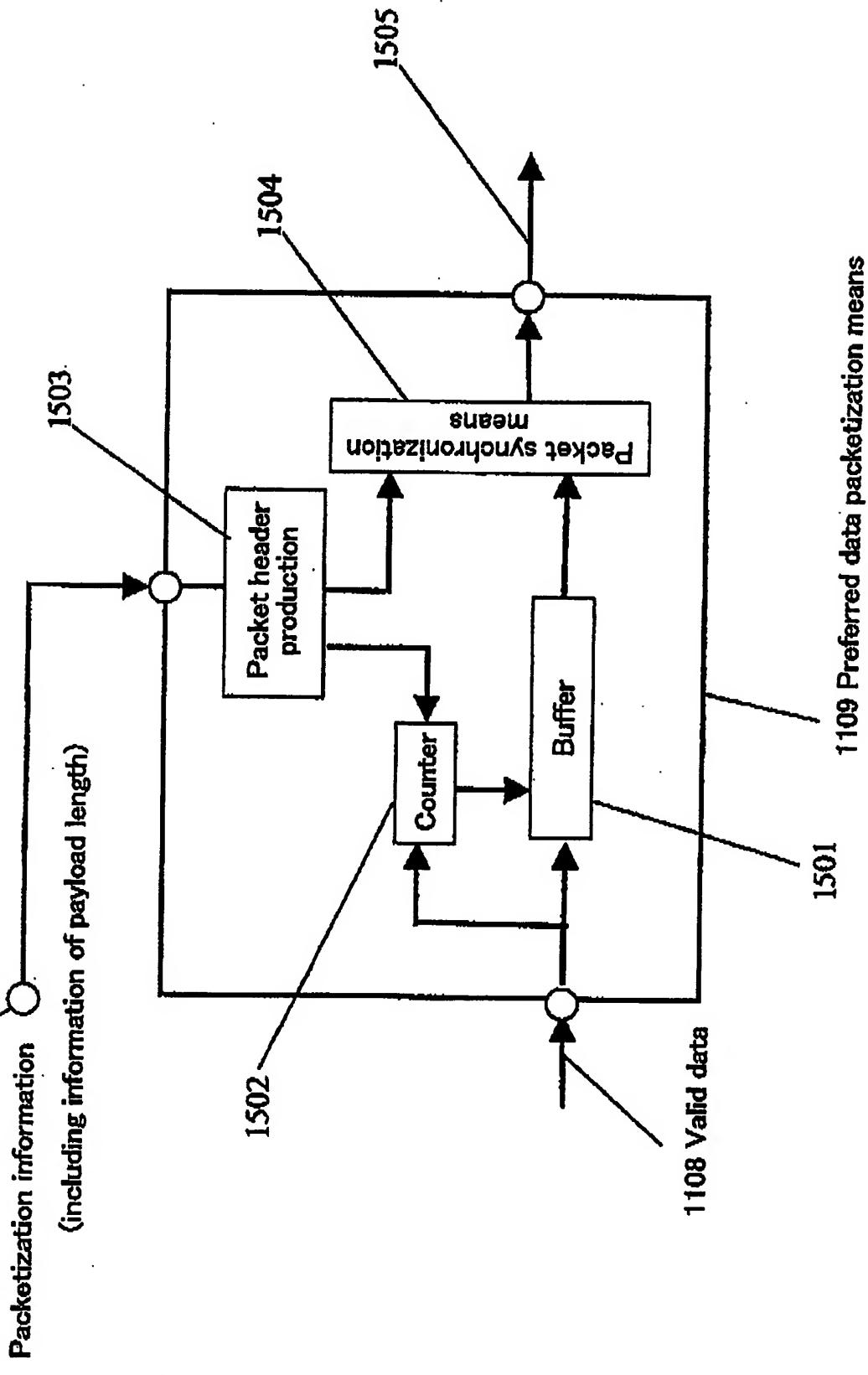
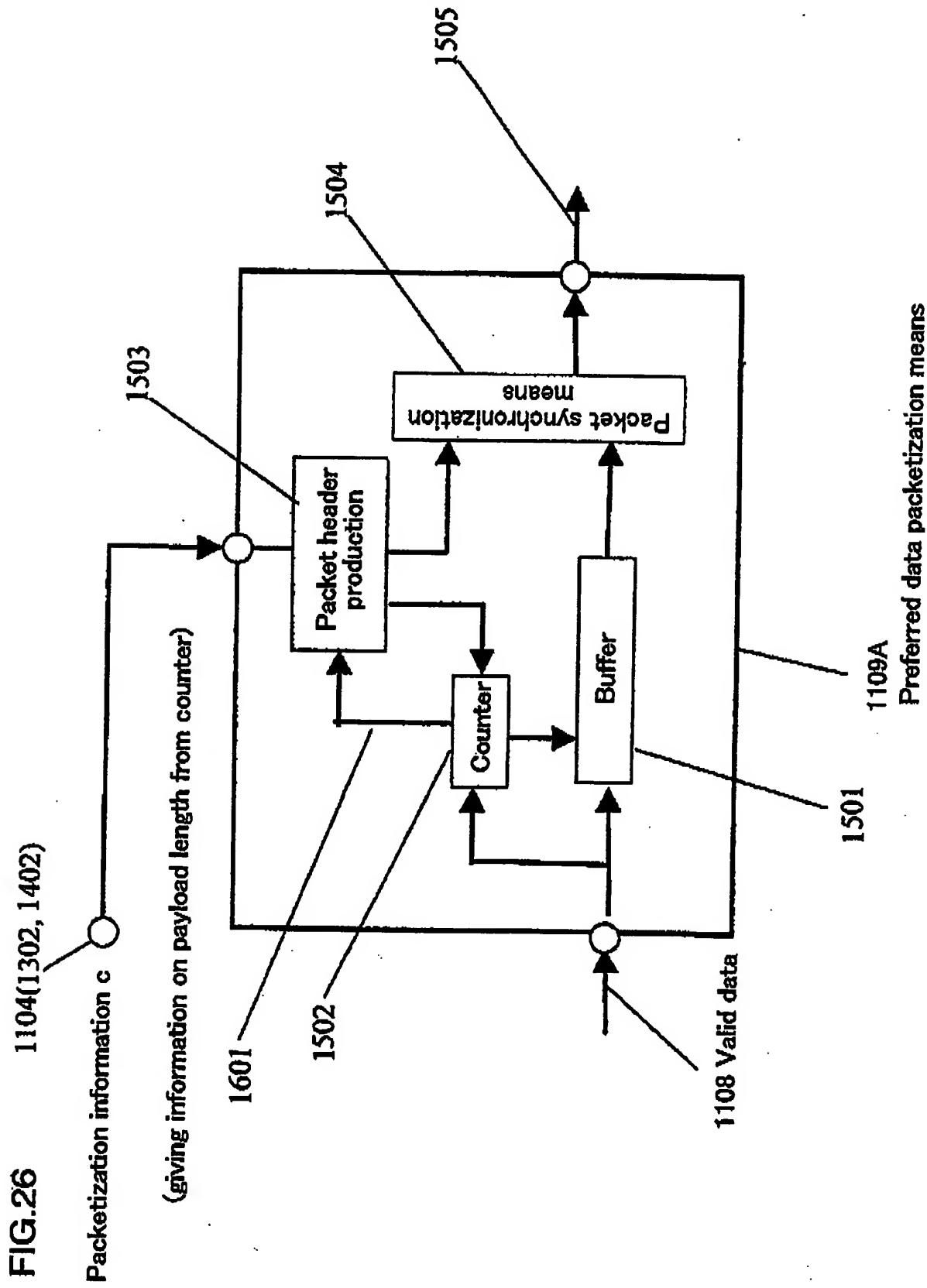


FIG.25





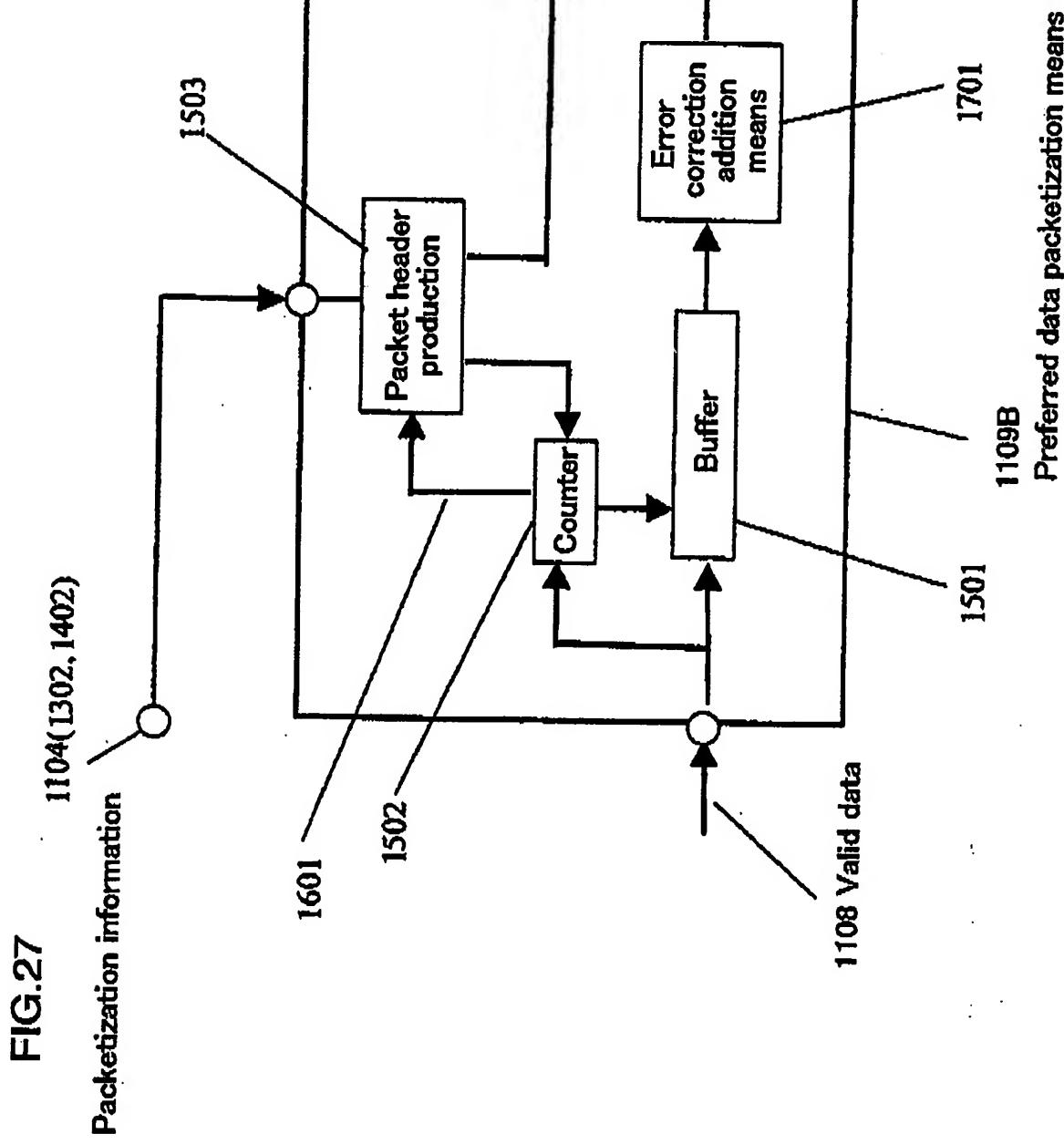


Fig. 28

Example where error correction addition  
means is Reed-Solomon code

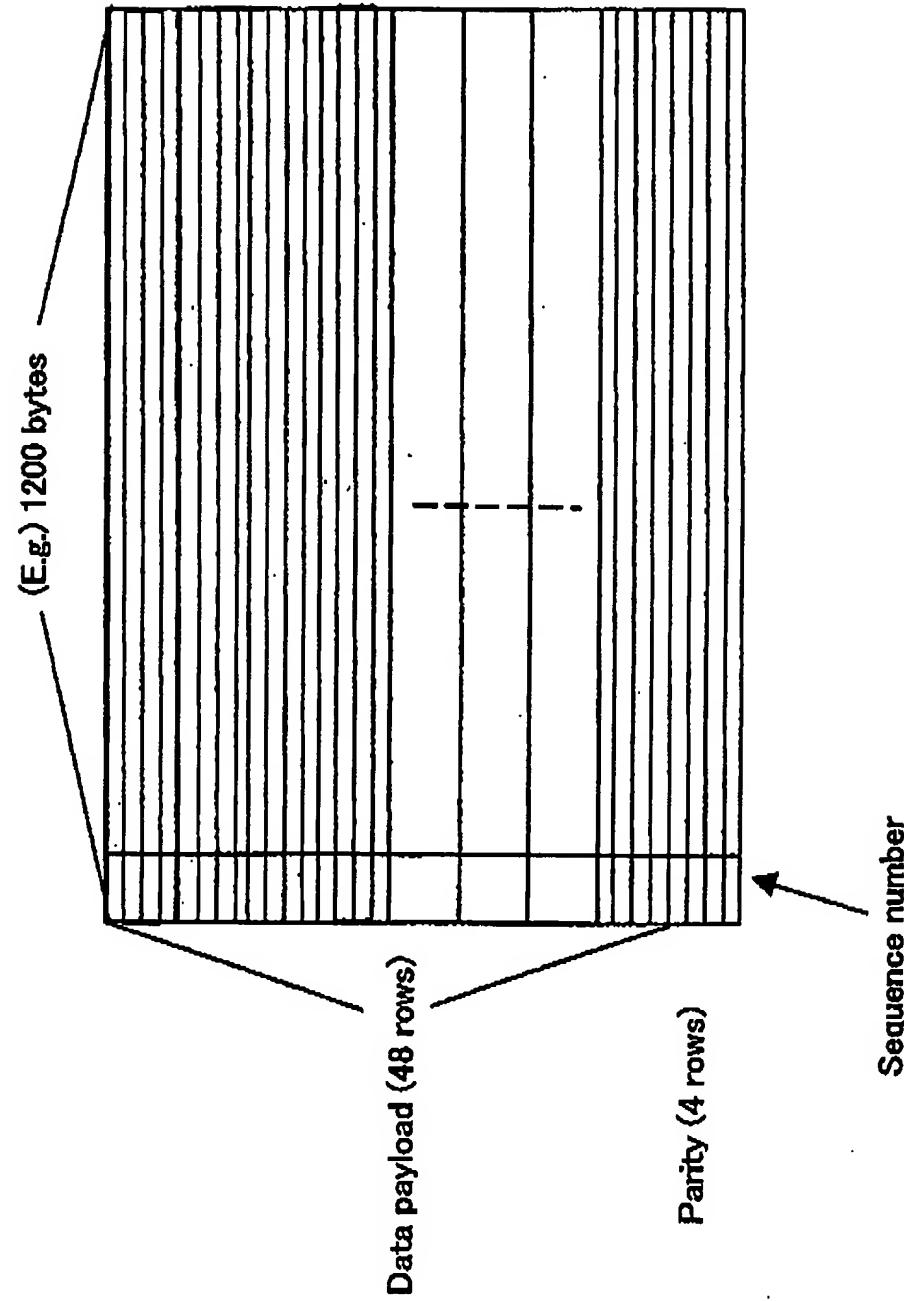
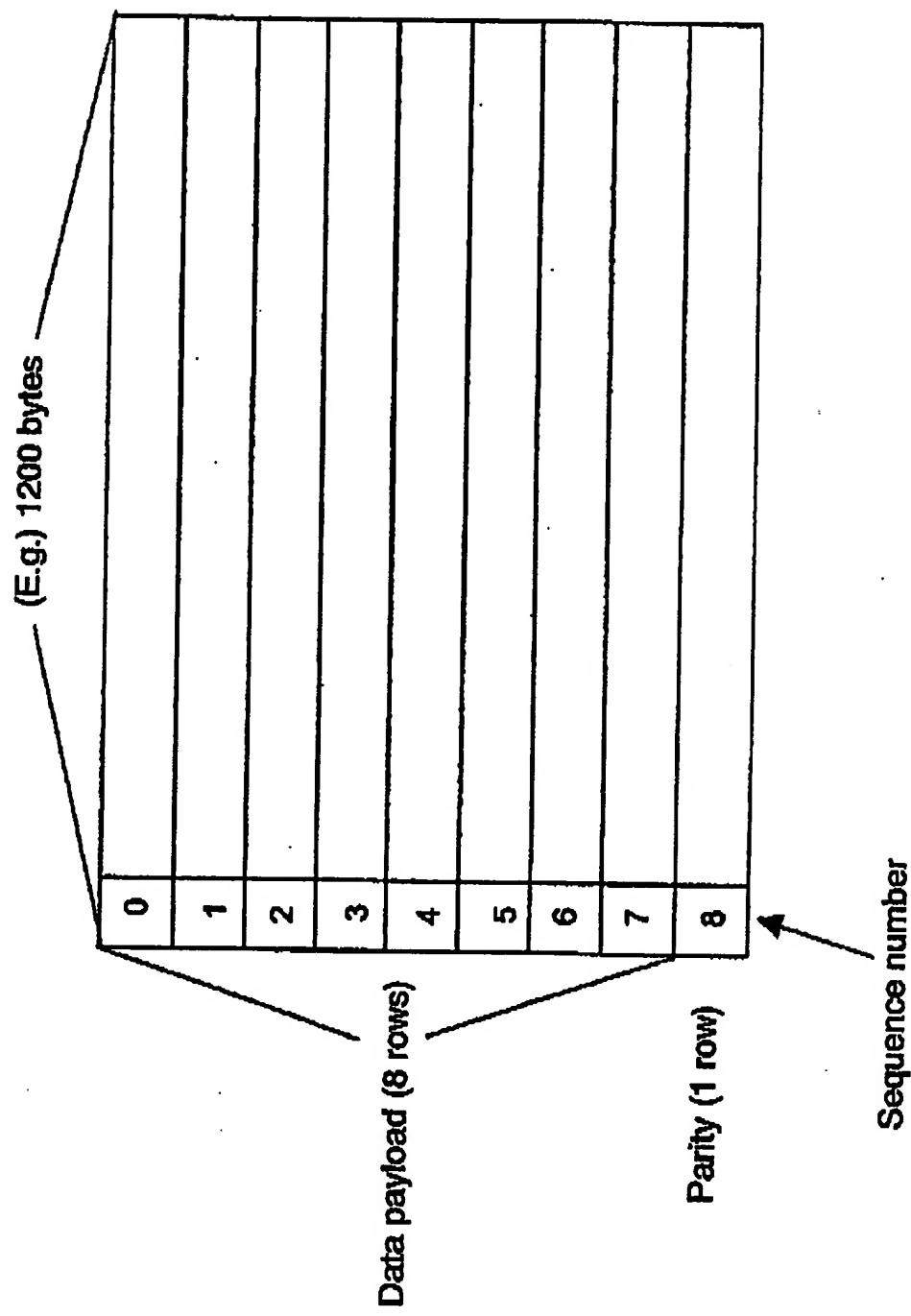
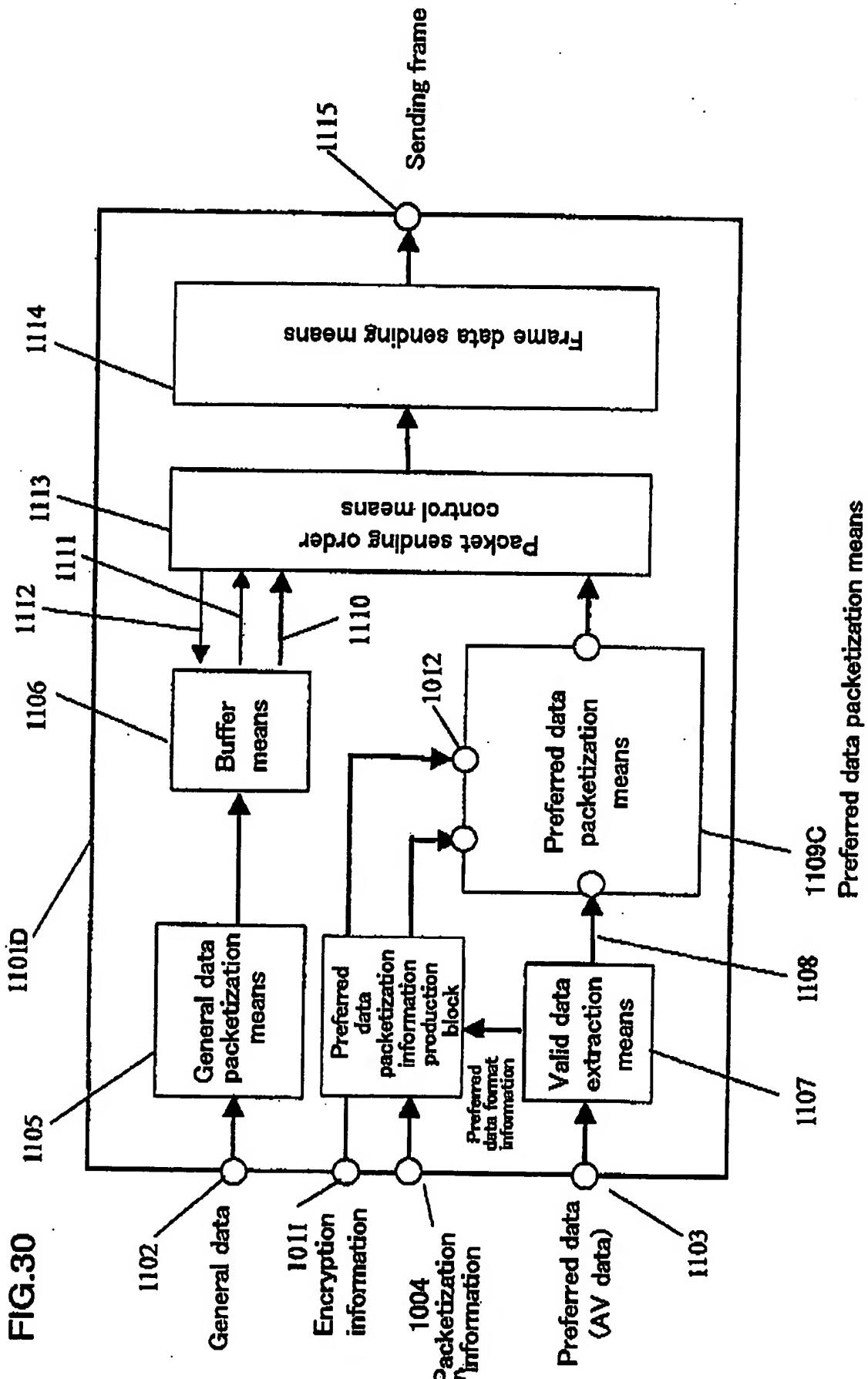


Fig. 29  
Example where error correction addition means is parity





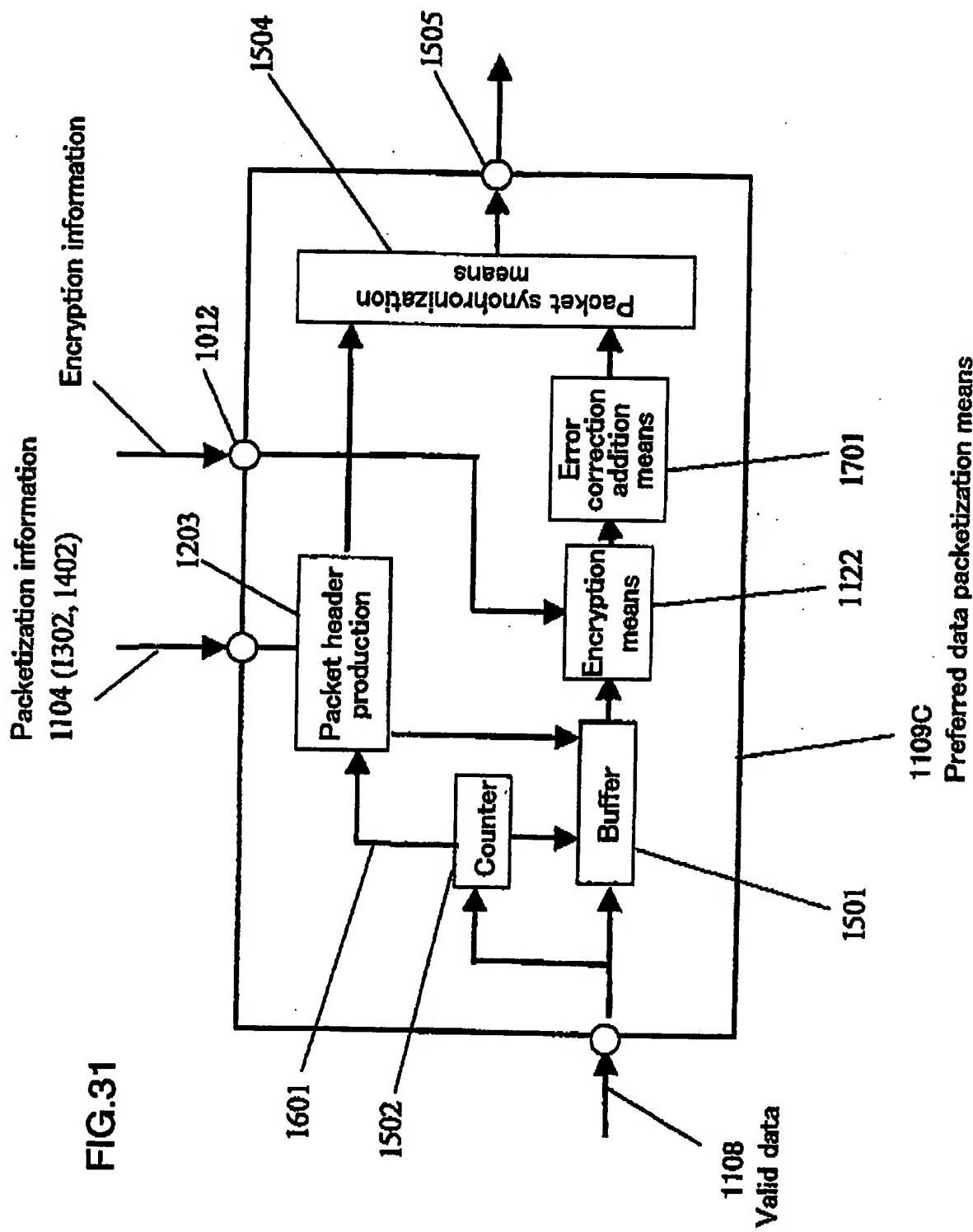


FIG. 32

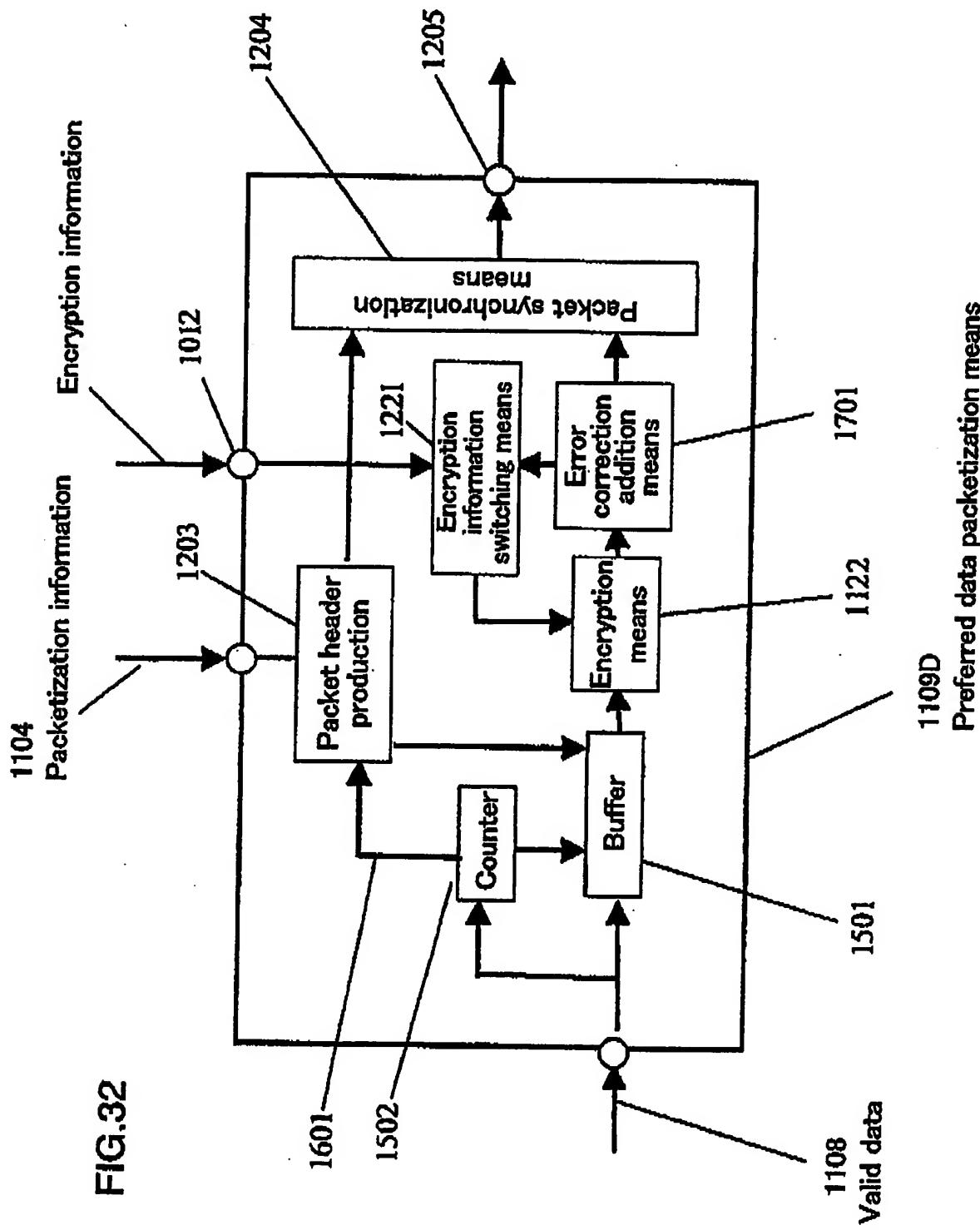
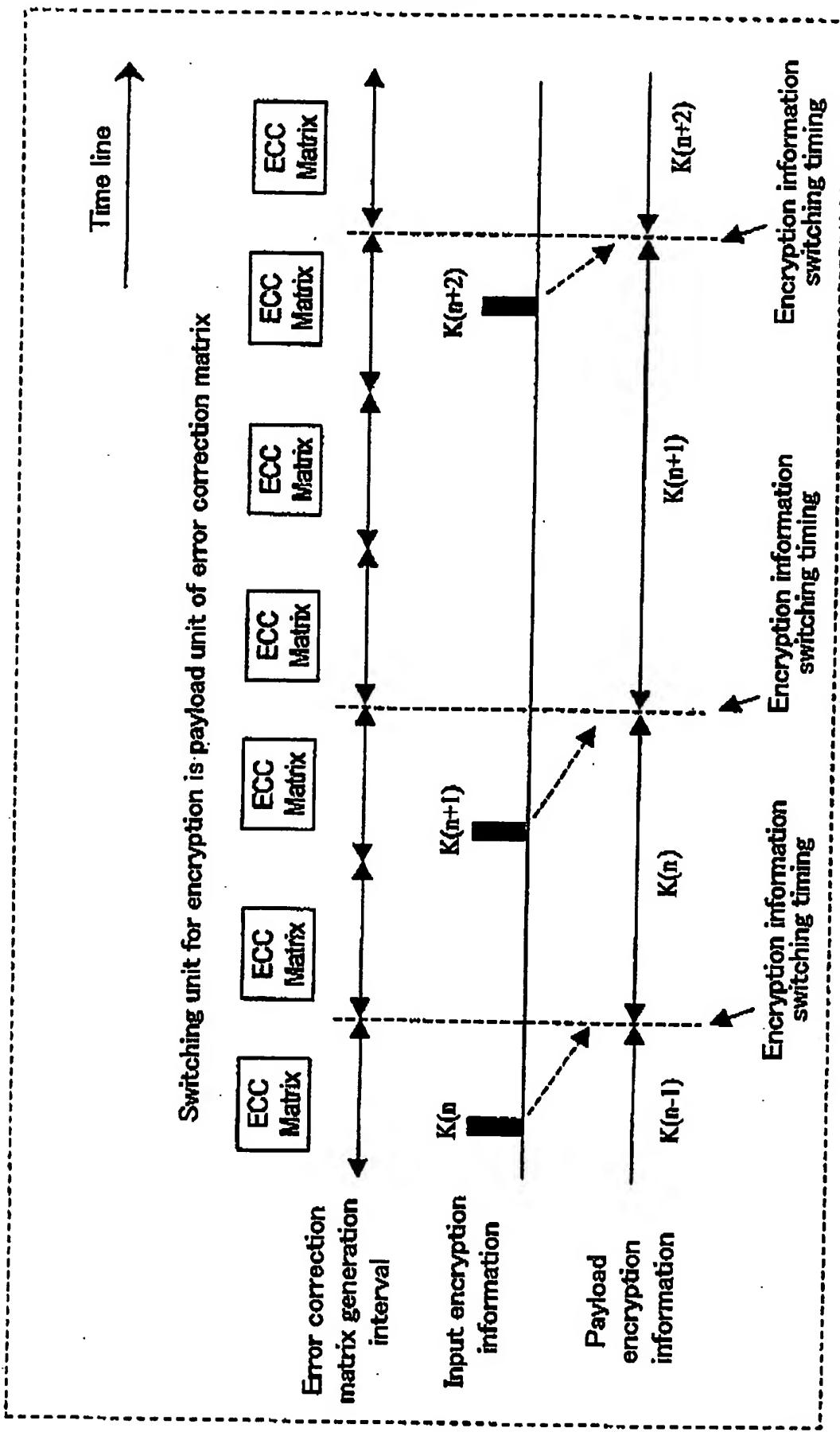
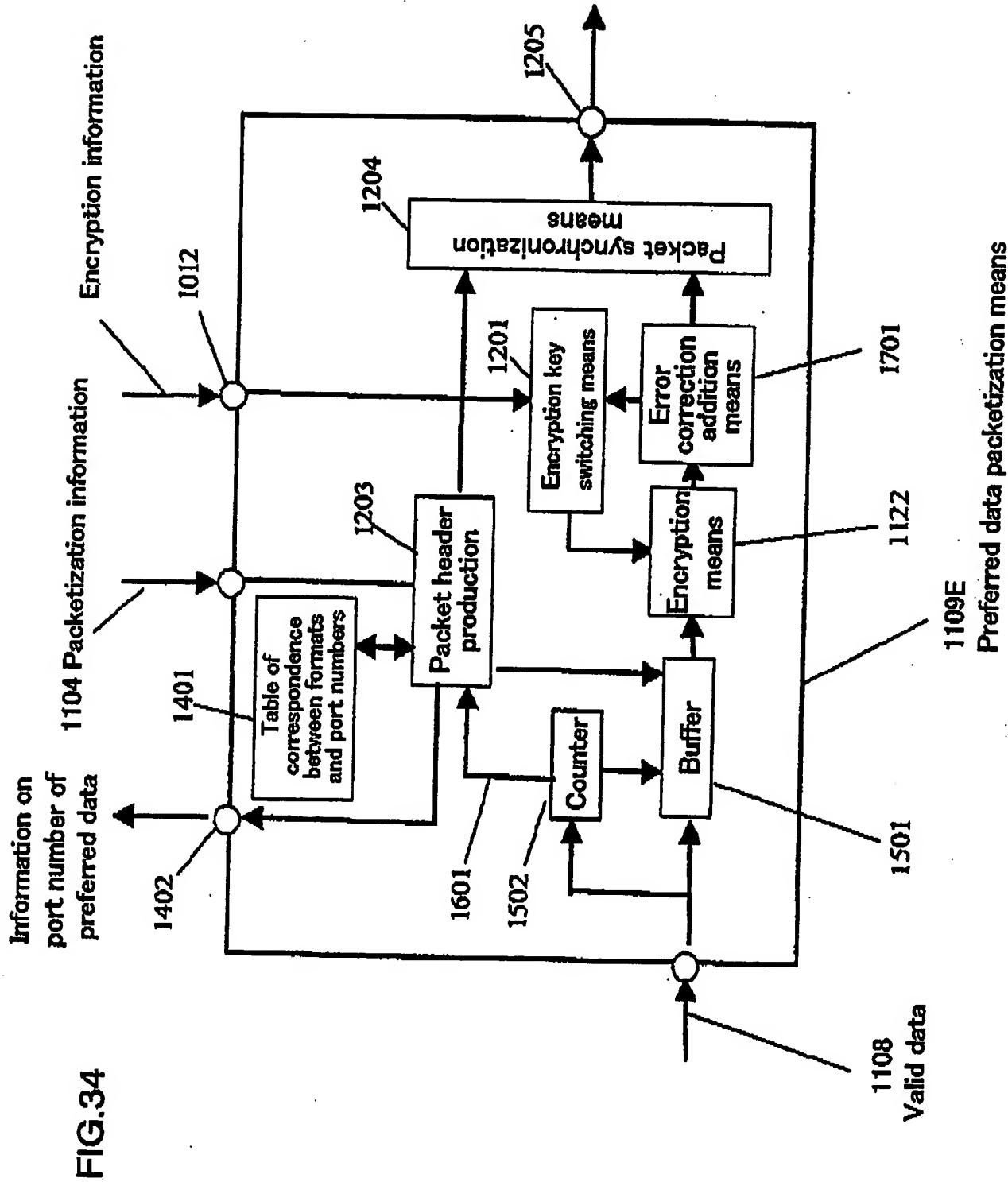
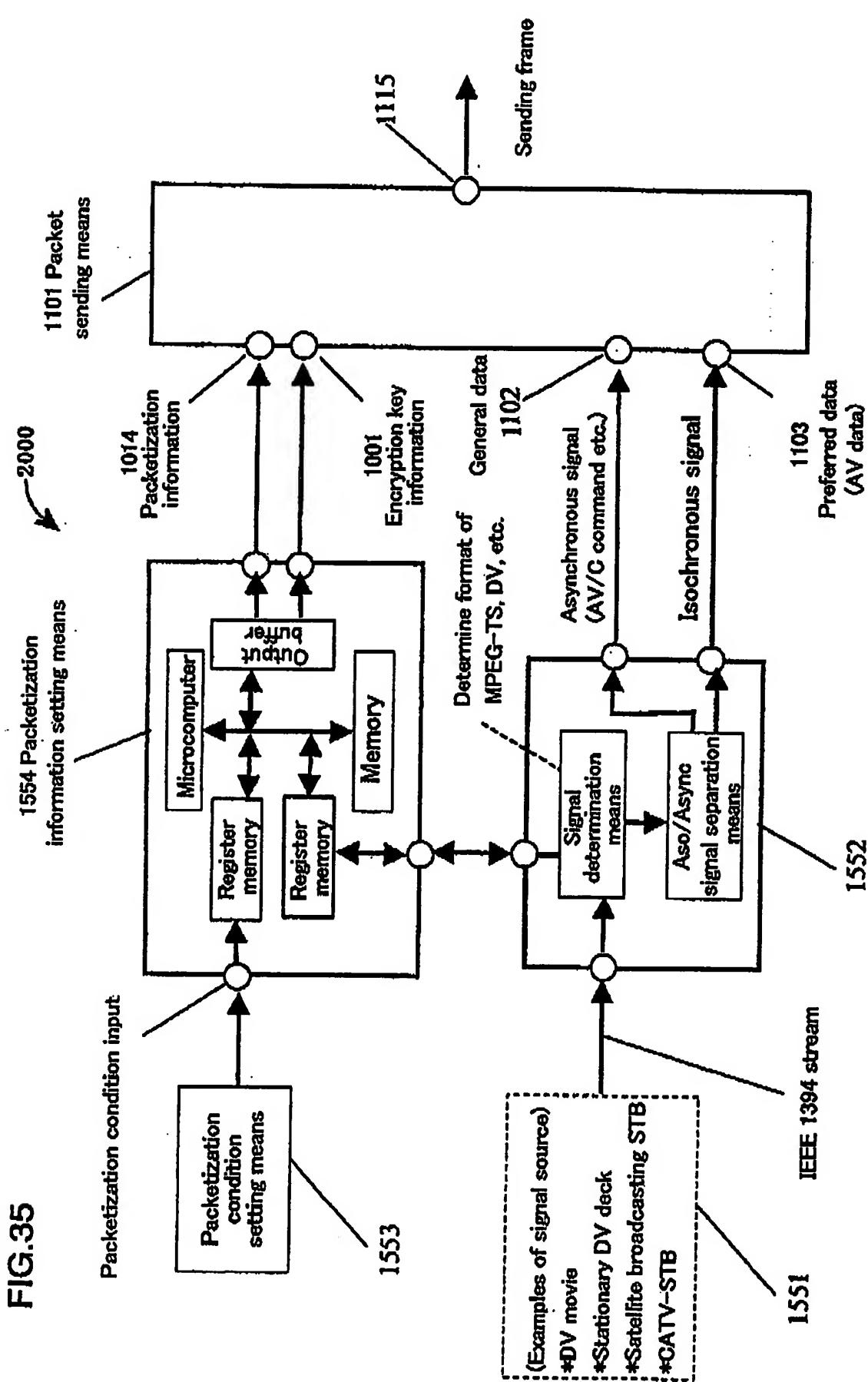


FIG.33







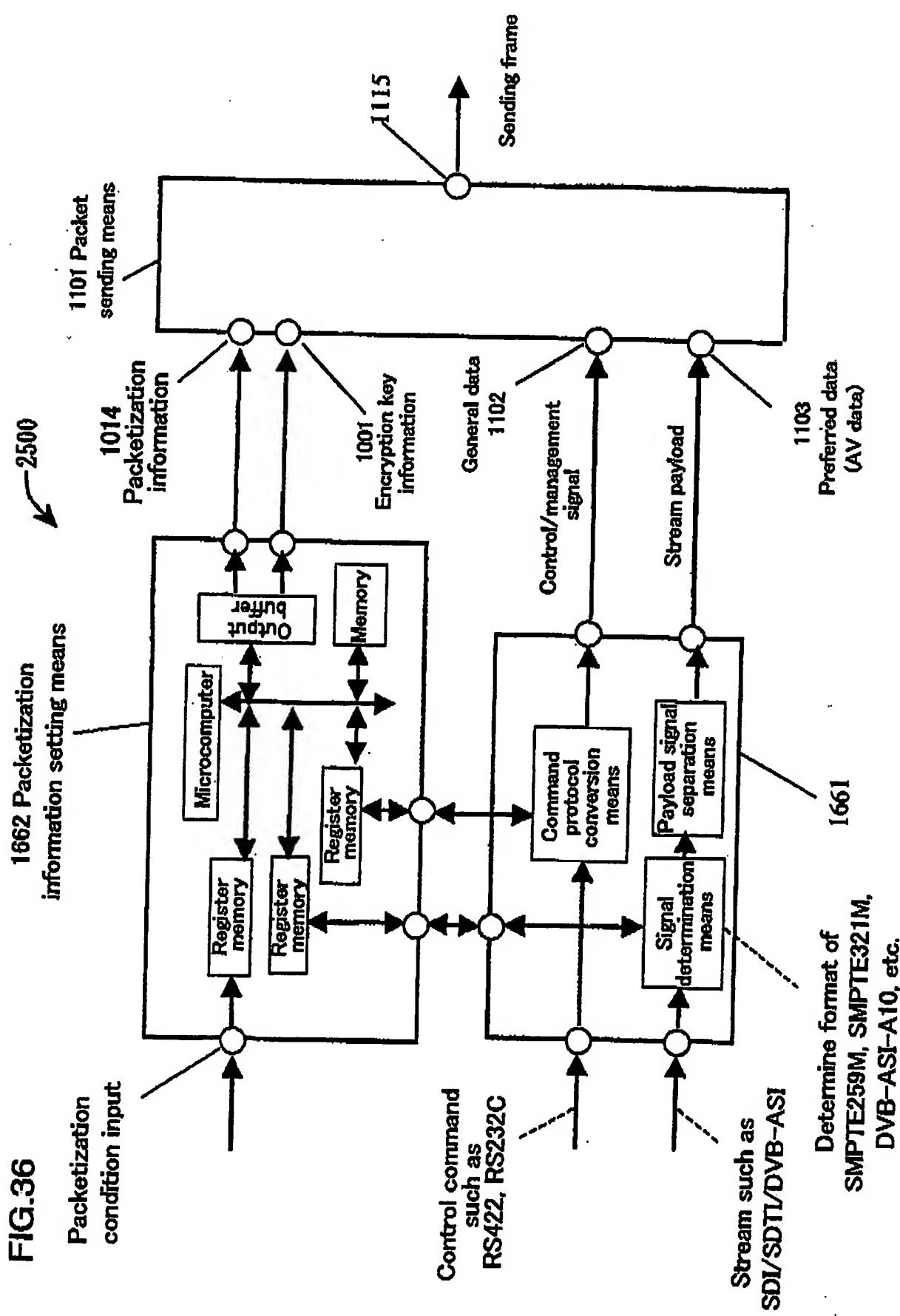
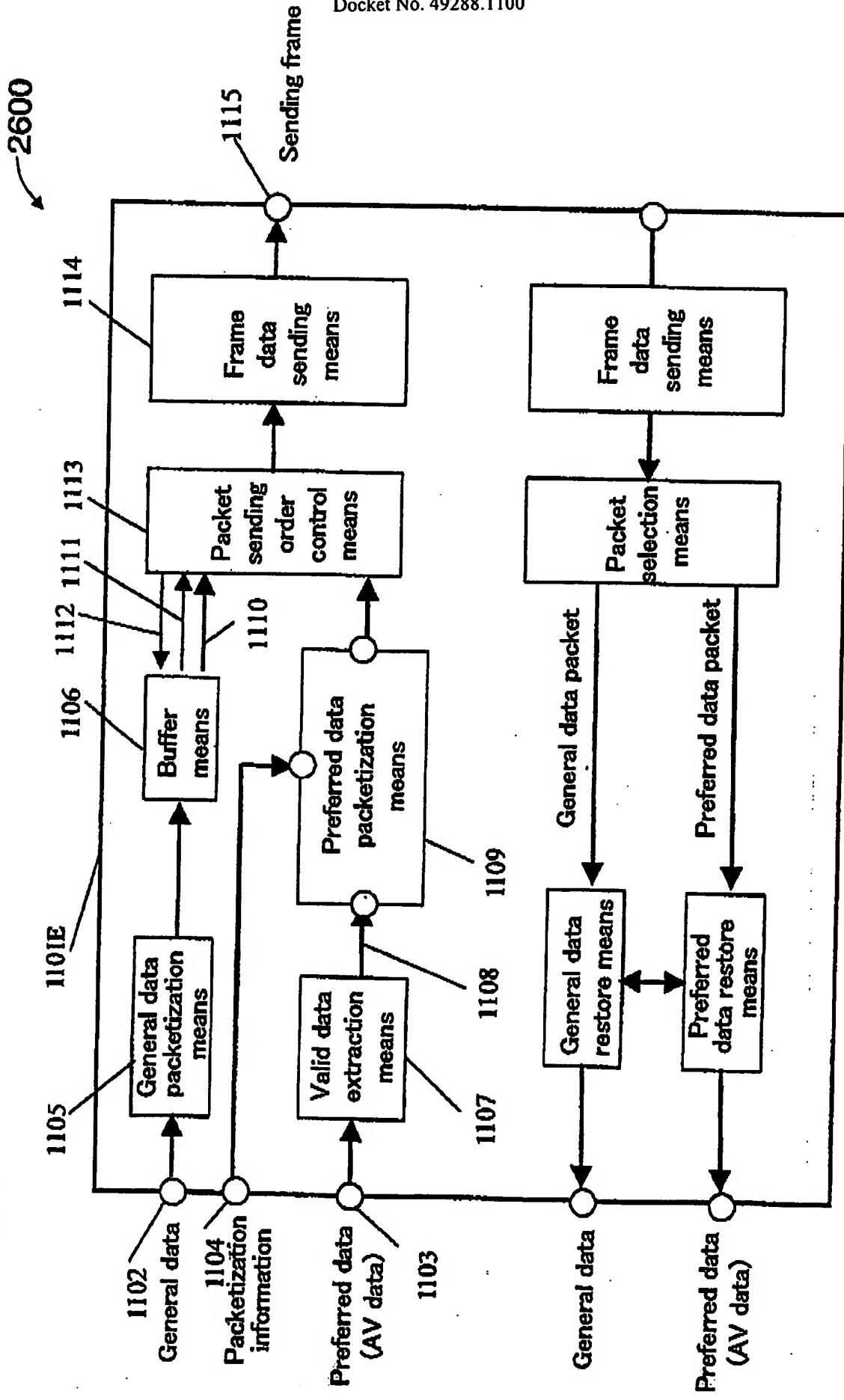


FIG.37



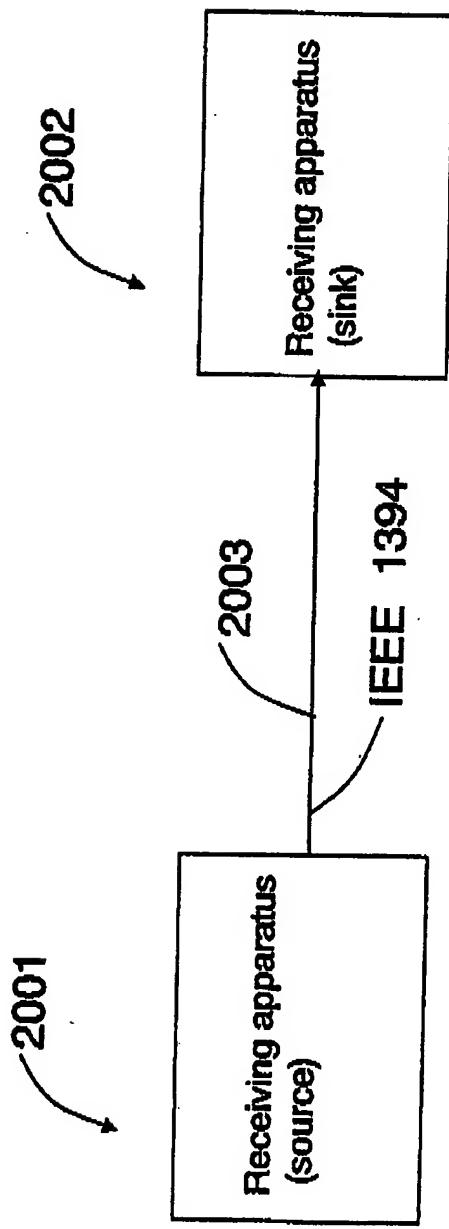


Fig. 38

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